



# MS\_7699 VER

## CPU: 10

AMD AM3 AM3+

## System Chipset:

AMD/ATI 760G/785G/880G

AMD/ATI RS710

## On Board Chipset:

FINTEK Super I/O -- F71868AD

LAN -- RLT8111E COLAY 8105

HD Codec --ALC887/892

UPD720200F1-USB 3.0

ASM1061 SATA 6G

BIOS -- SPI ROM 8M

## Main Memory:

DDR III X 4 (Max 32GB)

## Expansion Slots:

PCI-E X16 X1

PCI-E X1 X2

PCI 2.2 Slot X2

## Clock Generator:

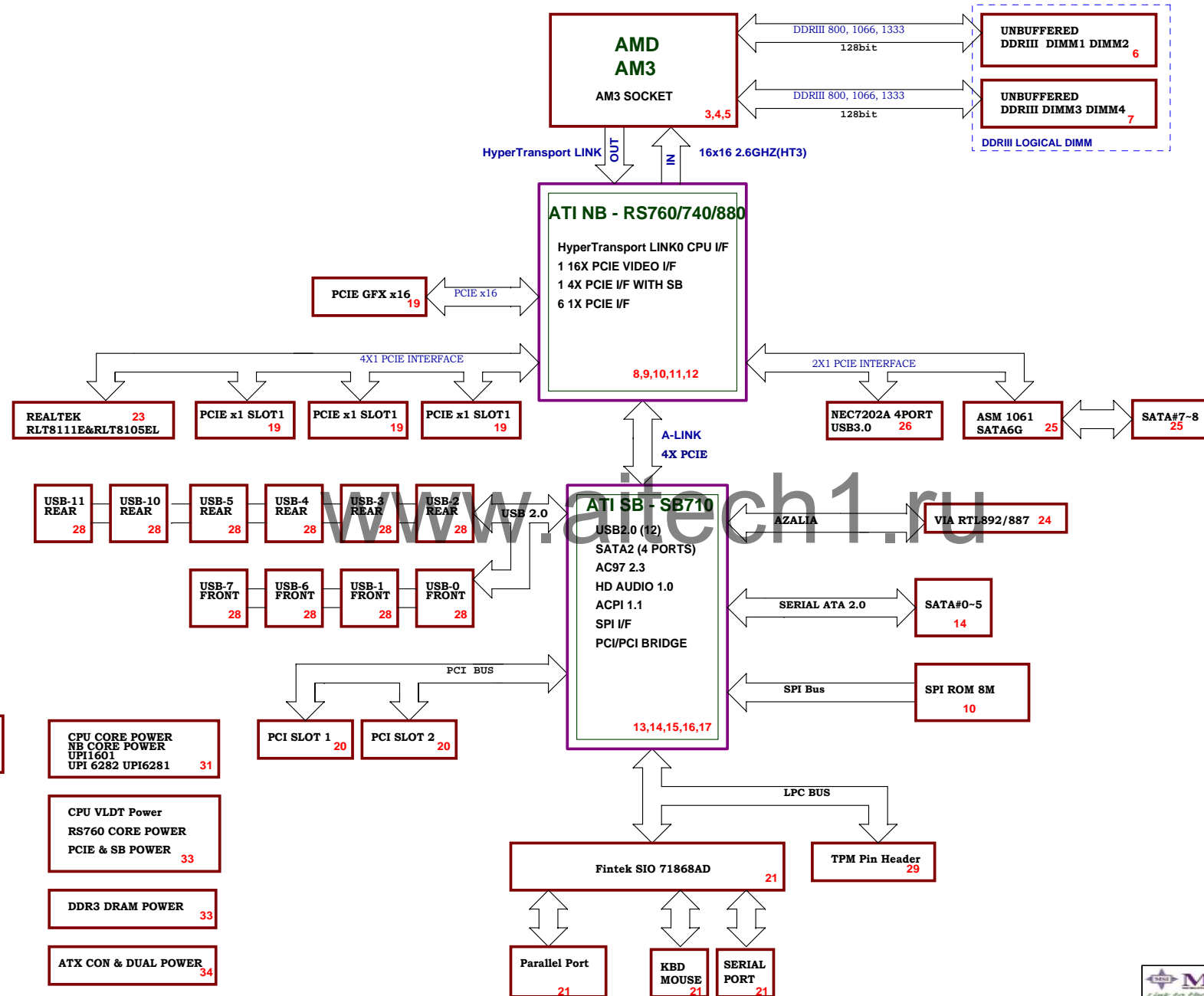
Controller--9LPRS477DKLFT

## PWM:

UPI1601

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# Project RS-740/760 BLOCK DIAGRAM

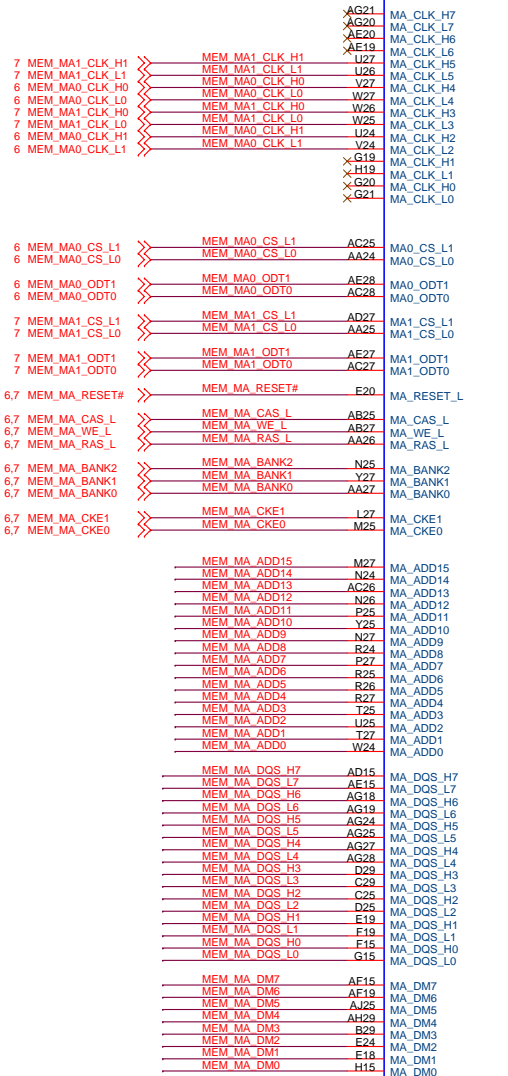




6,7 MEM\_MA\_DQS\_L[7..0] >> MEM\_MA\_DQS\_L[7..0]  
6,7 MEM\_MA\_DQS\_H[7..0] >> MEM\_MA\_DQS\_H[7..0]  
6,7 MEM\_MA\_DM[7..0] >> MEM\_MA\_DM[7..0]  
6,7 MEM\_MA\_ADD[15..0] >> MEM\_MA\_ADD[15..0]  
6,7 MEM\_MA\_DATA[63..0] >> MEM\_MA\_DATA[63..0]

6,7 MEM\_MB\_DQS\_L[7..0] >> MEM\_MB\_DQS\_L[7..0]  
6,7 MEM\_MB\_DQS\_H[7..0] >> MEM\_MB\_DQS\_H[7..0]  
6,7 MEM\_MB\_DM[7..0] >> MEM\_MB\_DM[7..0]  
6,7 MEM\_MB\_ADD[15..0] >> MEM\_MB\_ADD[15..0]  
6,7 MEM\_MB\_DATA[63..0] >> MEM\_MB\_DATA[63..0]

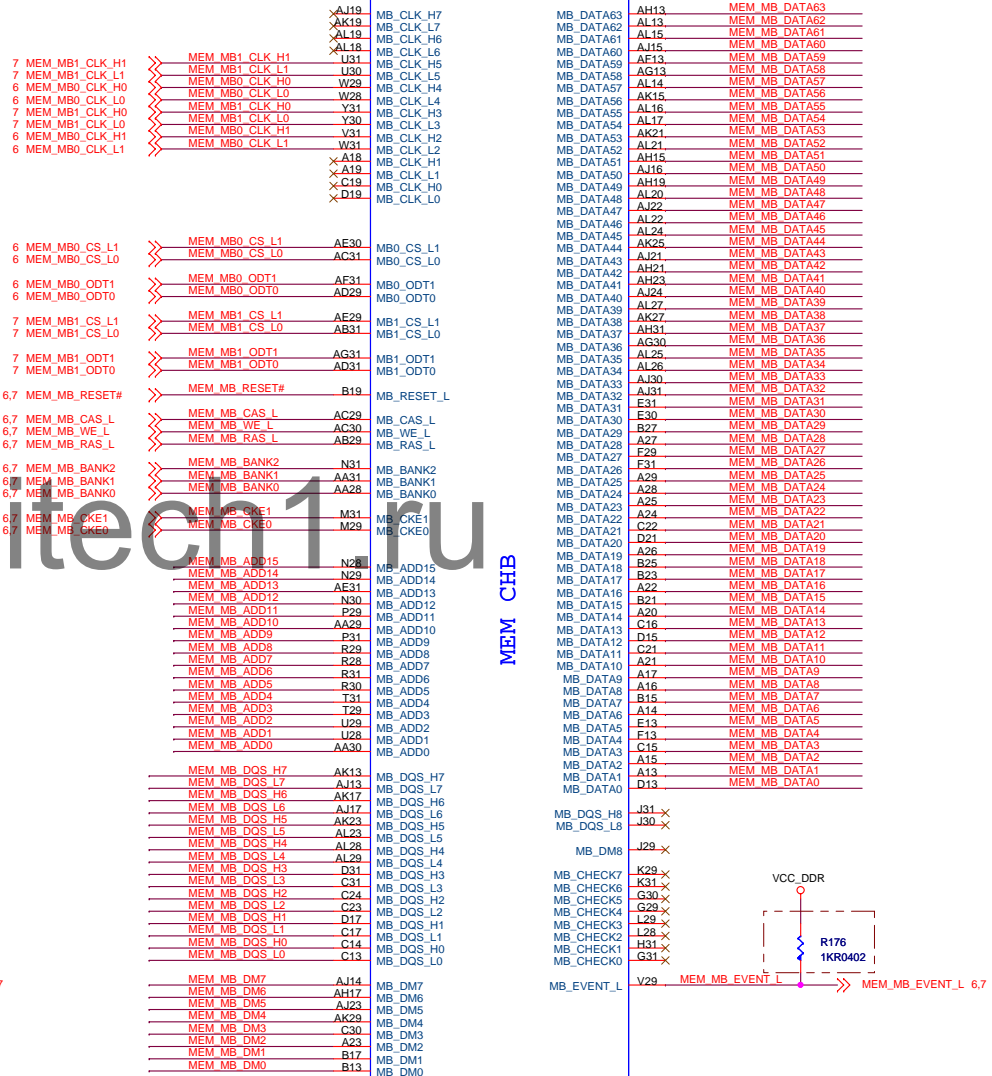
CPU1B



MEM\_CHA

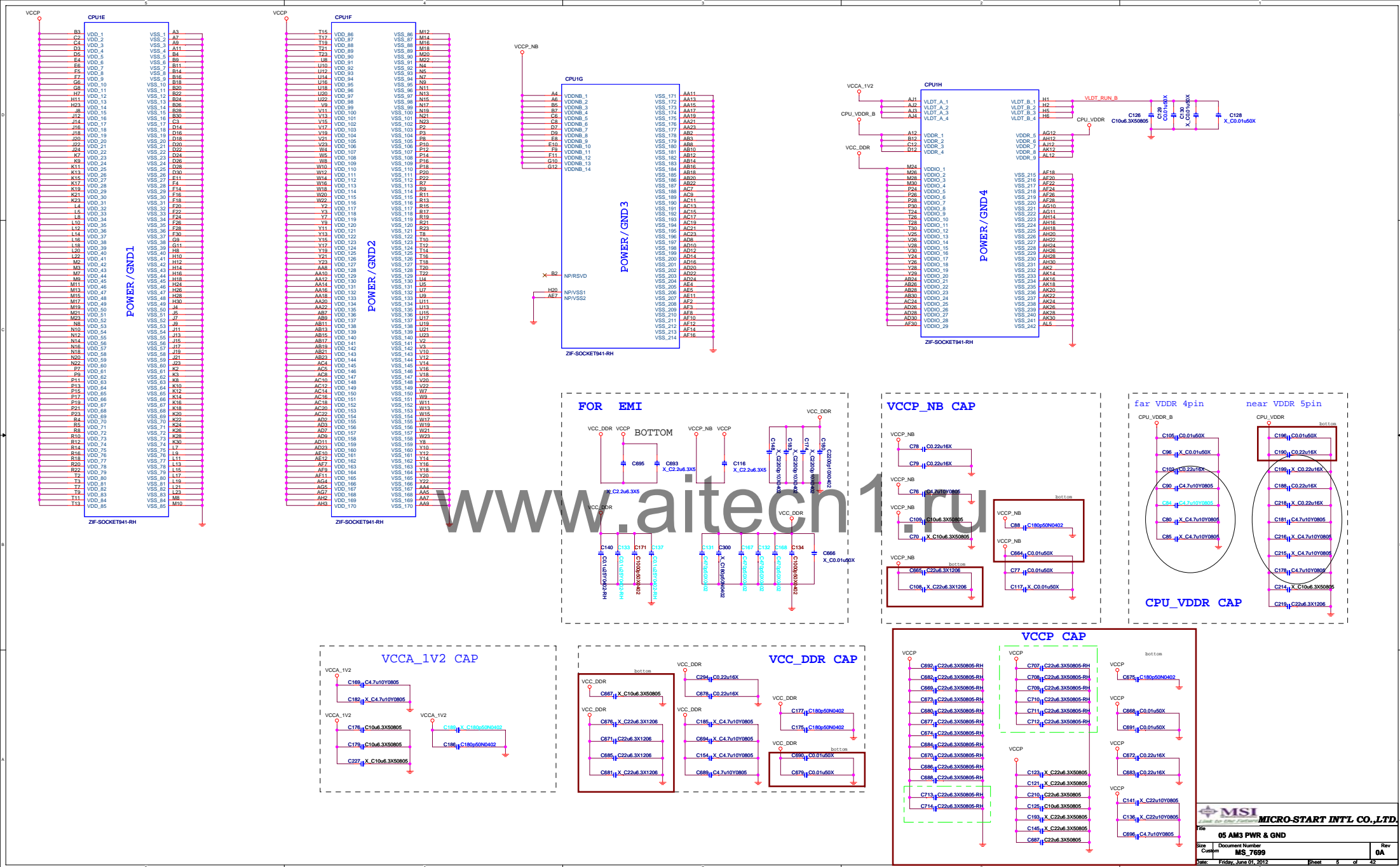
ZIF-SOCKET941-RH

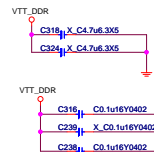
CPU1C



MEM\_CHB

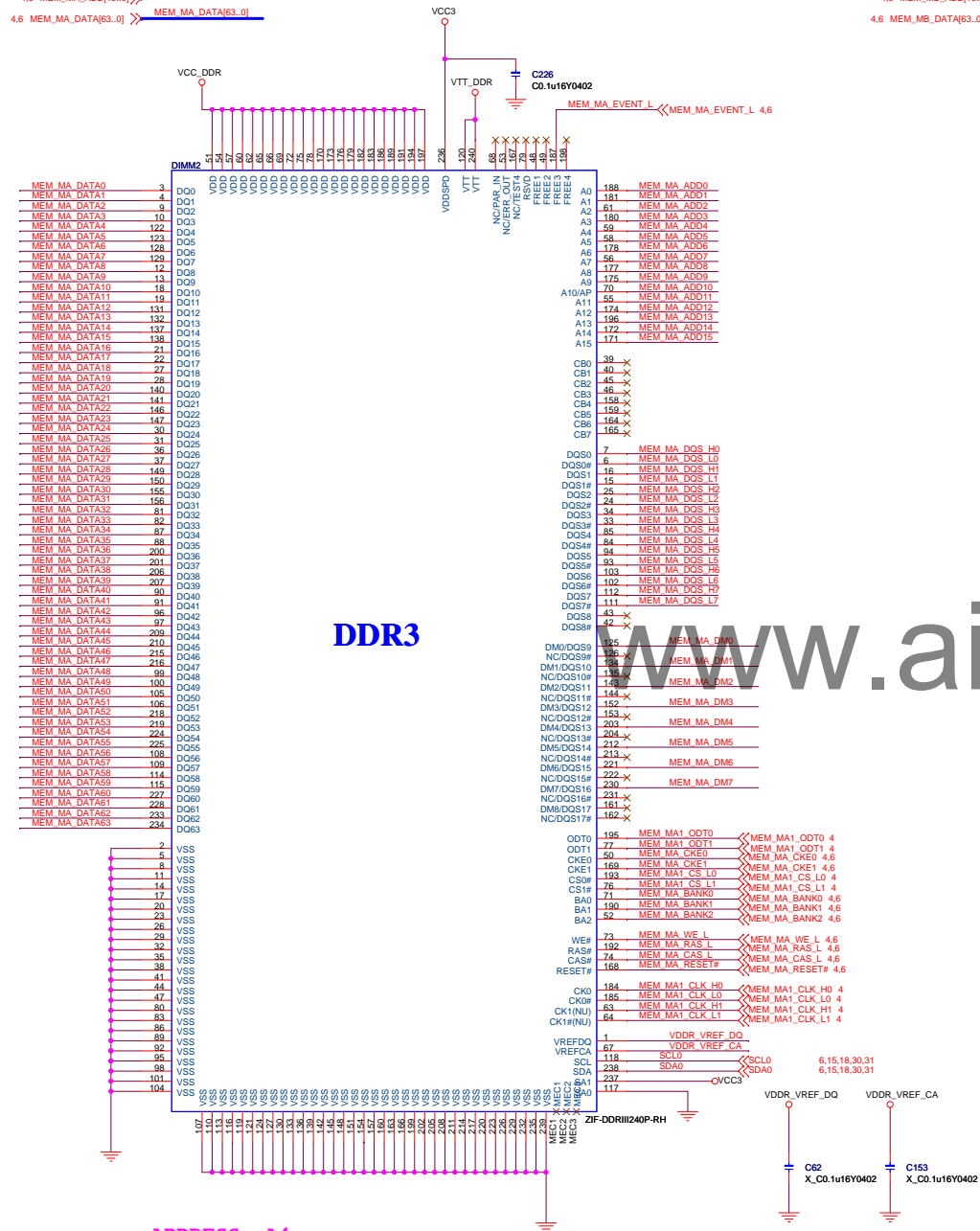
ZIF-SOCKET941-RH





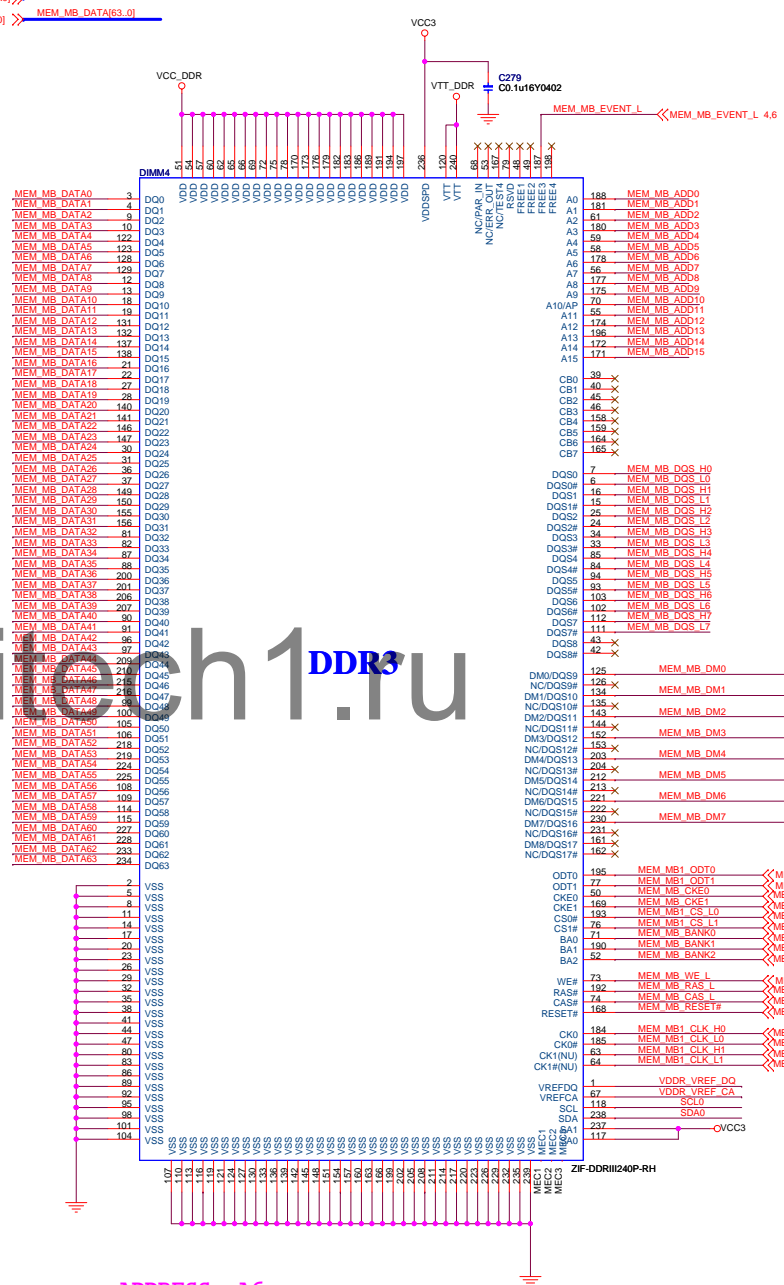


4.6 MEM\_MA\_DQS\_H[7..0] >> MEM\_MA\_DQS\_L[7..0]  
4.6 MEM\_MA\_DQS\_L[7..0] >> MEM\_MA\_DQS\_H[7..0]  
4.6 MEM\_MA\_DM[7..0] >> MEM\_MA\_ADD[15..0]  
4.6 MEM\_MA\_ADD[15..0] >> MEM\_MA\_ADD[15..0]  
4.6 MEM\_MA\_DATA[63..0] >> MEM\_MA\_DATA[63..0]

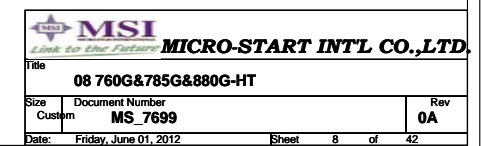


ADDRESS A4

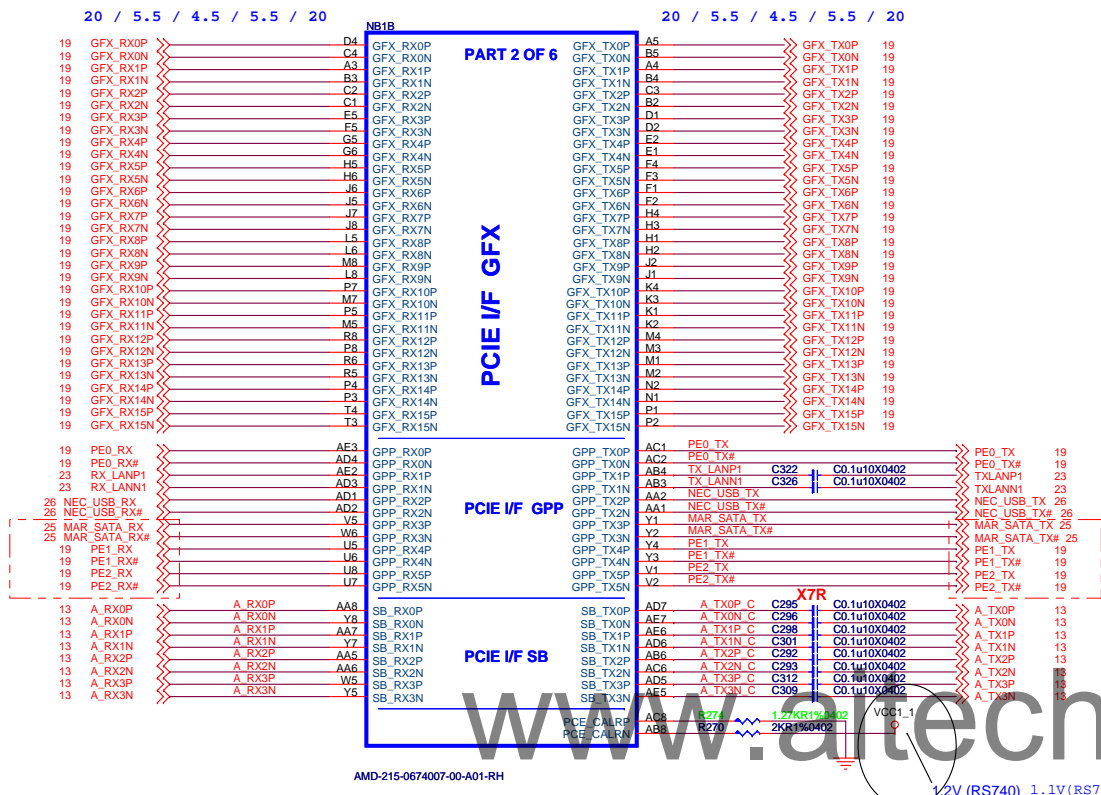
4.6 MEM\_MB\_DQS\_L[7..0] >> MEM\_MB\_DQS\_L[7..0]  
4.6 MEM\_MB\_DQS\_H[7..0] >> MEM\_MB\_DQS\_H[7..0]  
4.6 MEM\_MB\_DM[7..0] >> MEM\_MB\_ADD[15..0]  
4.6 MEM\_MB\_ADD[15..0] >> MEM\_MB\_ADD[15..0]  
4.6 MEM\_MB\_DATA[63..0] >> MEM\_MB\_DATA[63..0]



ADDRESS A6







AMD-215-0674007-00-A01-RH

RX780/RS740/RS780 GPP difference table

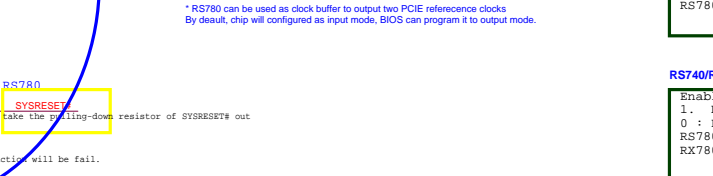
	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

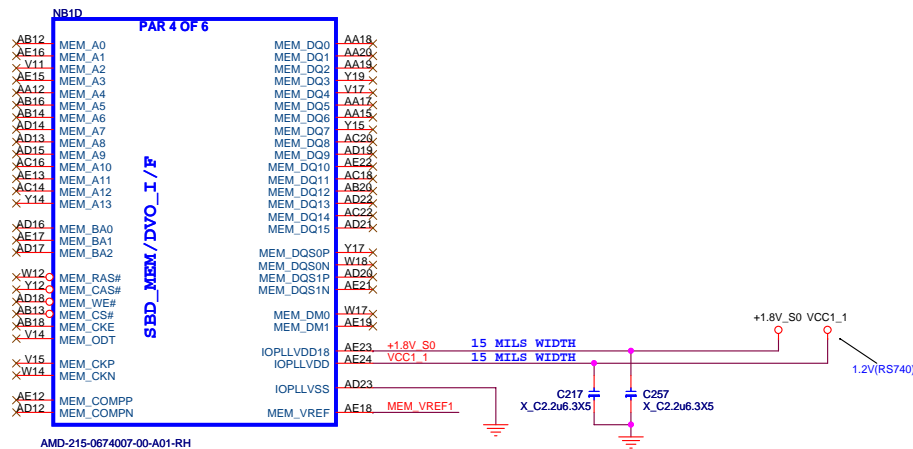
RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5



RX740/RS740/RS780 JTAG PIN MAPPING		
	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RS3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

\_\_\_\_\_



FOR RS780, R148, R162, C203 and C202 will be populated.

AMD: Please let MEM\_VREF short to GND when Sideport is not used.

## RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX\_CAL, place close to pin C8

10 RS740\_DFT\_GPIO1 >> R278 150R0402

10,29 VSYNC# >> R262 3KR0402  
R265 X 3KR0402  
10 RS740\_DFT\_GPIO5 >> R275 X 3KR0402

### RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

10 RS740\_DFT\_GPIO0 >> R286 X 3KR0402  
10,29 HSYNC# >> R261 X 3KR0402  
R256 3KR0402

Have not side port memory, AMD suggest HSYNC pull up to VCC3

### RX780/RS780: STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

### RS740/RX780/RS780: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EEPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS740: pin DFT\_GPIO1

RS780: pin SUS\_STAT#

### RS740/RX780/RS780: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

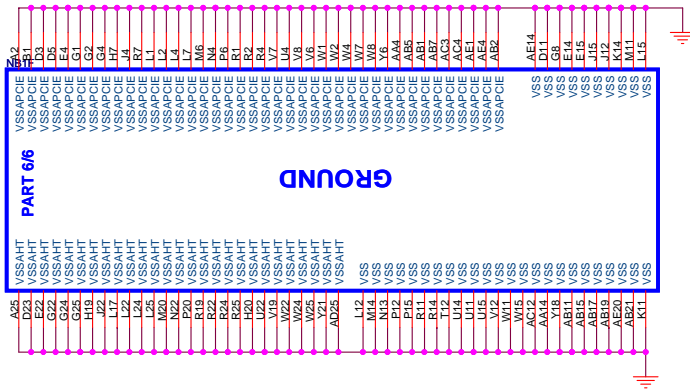
Enables the Test Debug Bus using GPIO and/or memory IO  
1 : Disable (RS740/RS780); Enable (RX780)  
0 : Enable (RS740/RS780); Disable (RX780)  
RS740: pin DFT\_GPIO5

RS780: pin VSYNC

Enables Side port memory  
1. Disable (RS740/RS780)  
0 : Enable (RS740/RS780)  
RS740: pin DFT\_GPIO0  
RS780: pin HSYNC

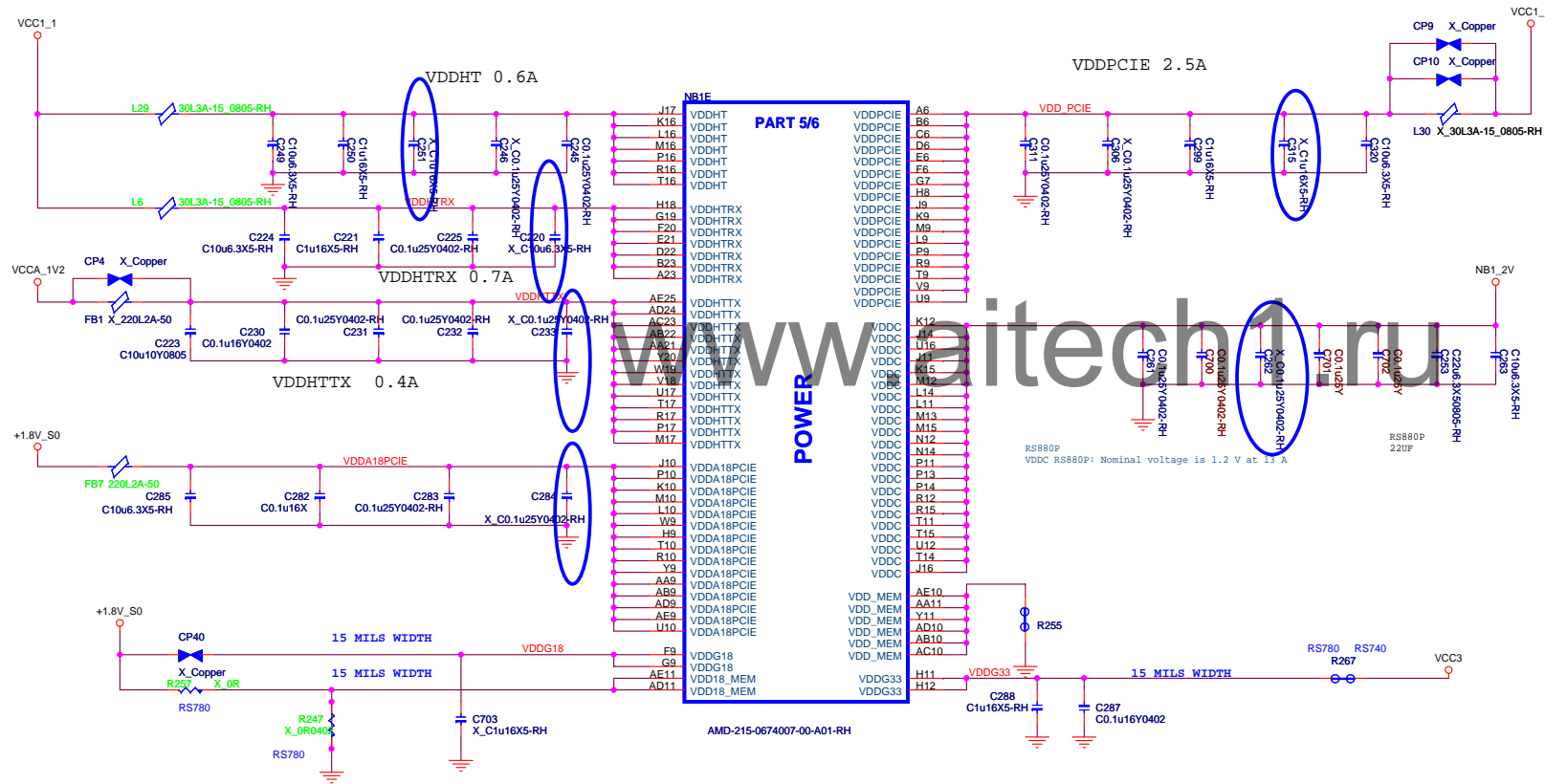
Enables Test debug bus using PCIE bus  
1. Disable (can be enabled thru nbcfg register)  
0 : Enable  
RS780: configurable thru register setting only  
RS740: Not supported

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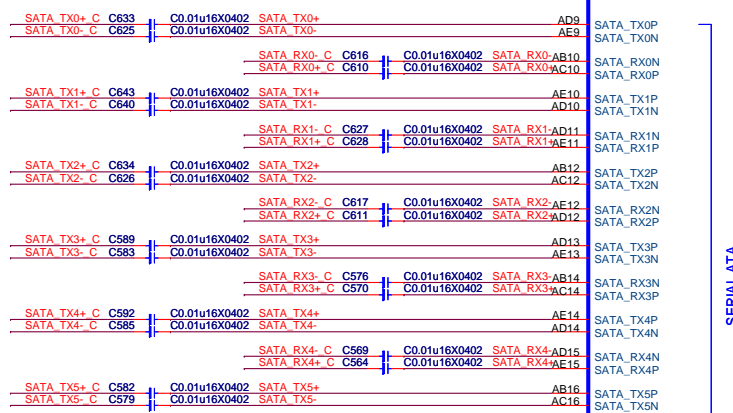
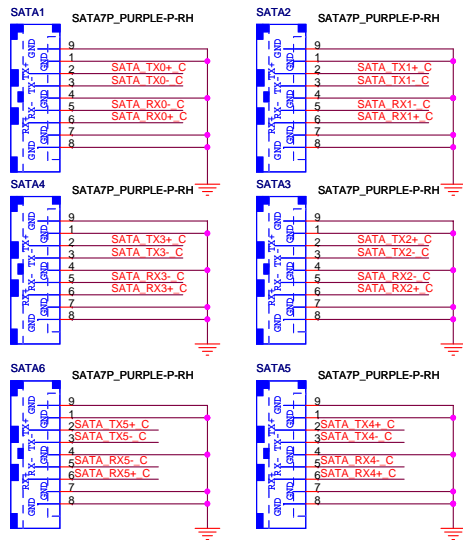
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC

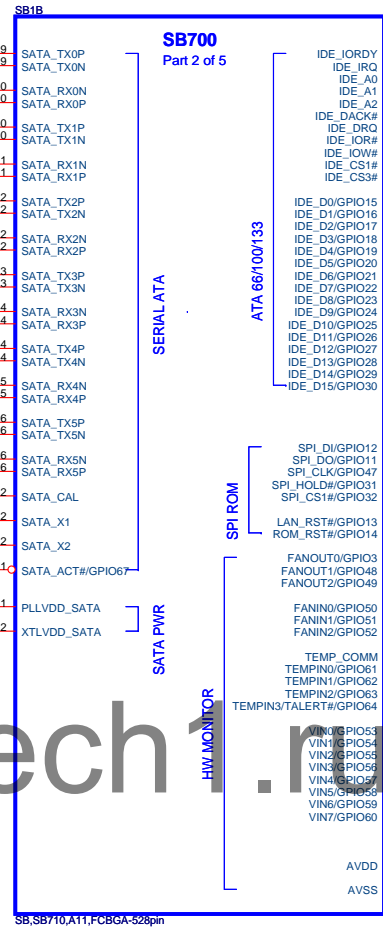
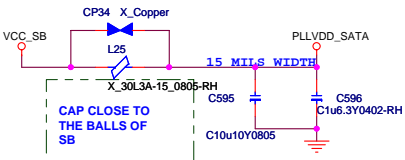
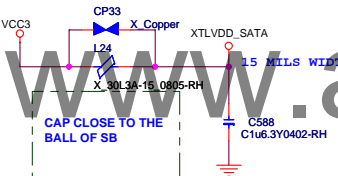
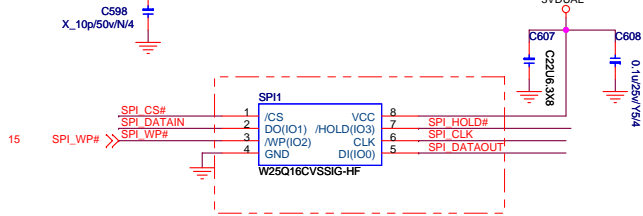
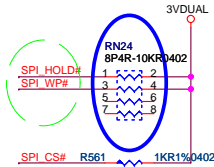
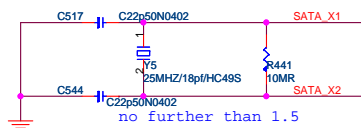


VDD18\_MEM  
RS780 without Side-Port/RX781/RS780C/RS780L/RS780MC:  
Connected to GND plane (preferred) or connected to 1.8V\_S0 power rail.





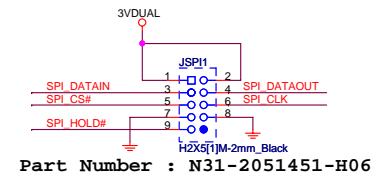
34 SATA\_LED << SATA LED



# SPI FLASH MEMORY

Place close to SPI ROM

# SPI DEBUG PORT



SPI ROM change to M31-25Q8003-W03



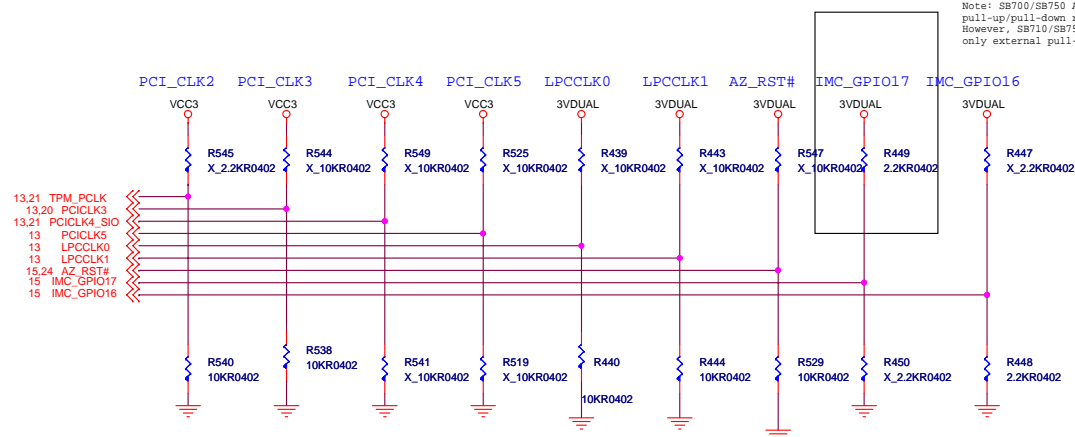






## REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK



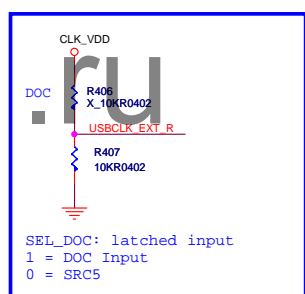
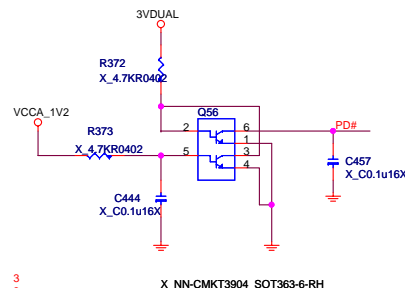
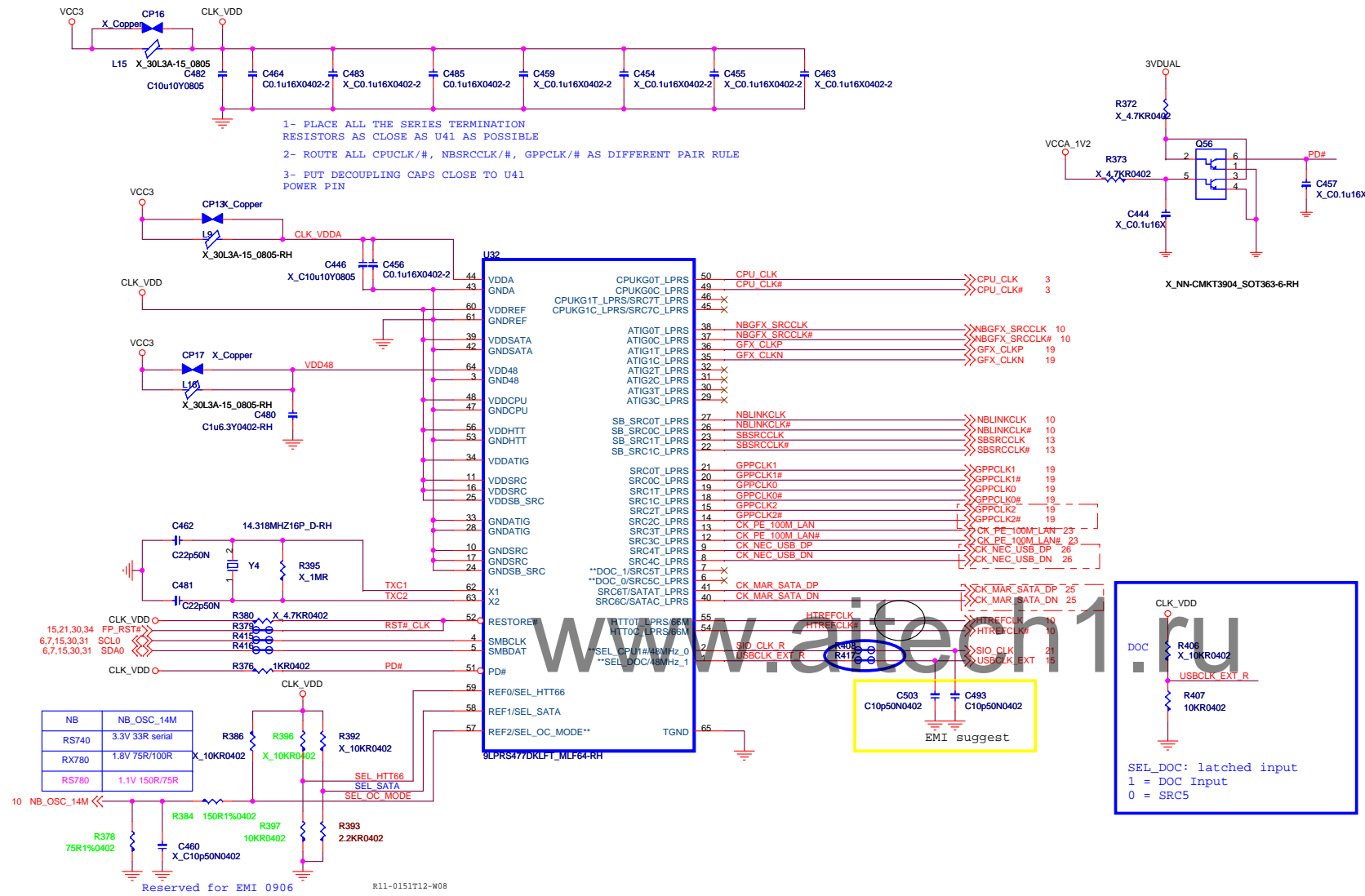
Note: SB700/SB750 A12 IMC\_GPIO[17:16] require external pull-up/pull-down resistors to configure ROM straps. However, SB710/SB750 A14 IMC\_GPIO[17:16] require only external pull-down resistors to configure ROM straps.

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

## DEBUG STRAPS

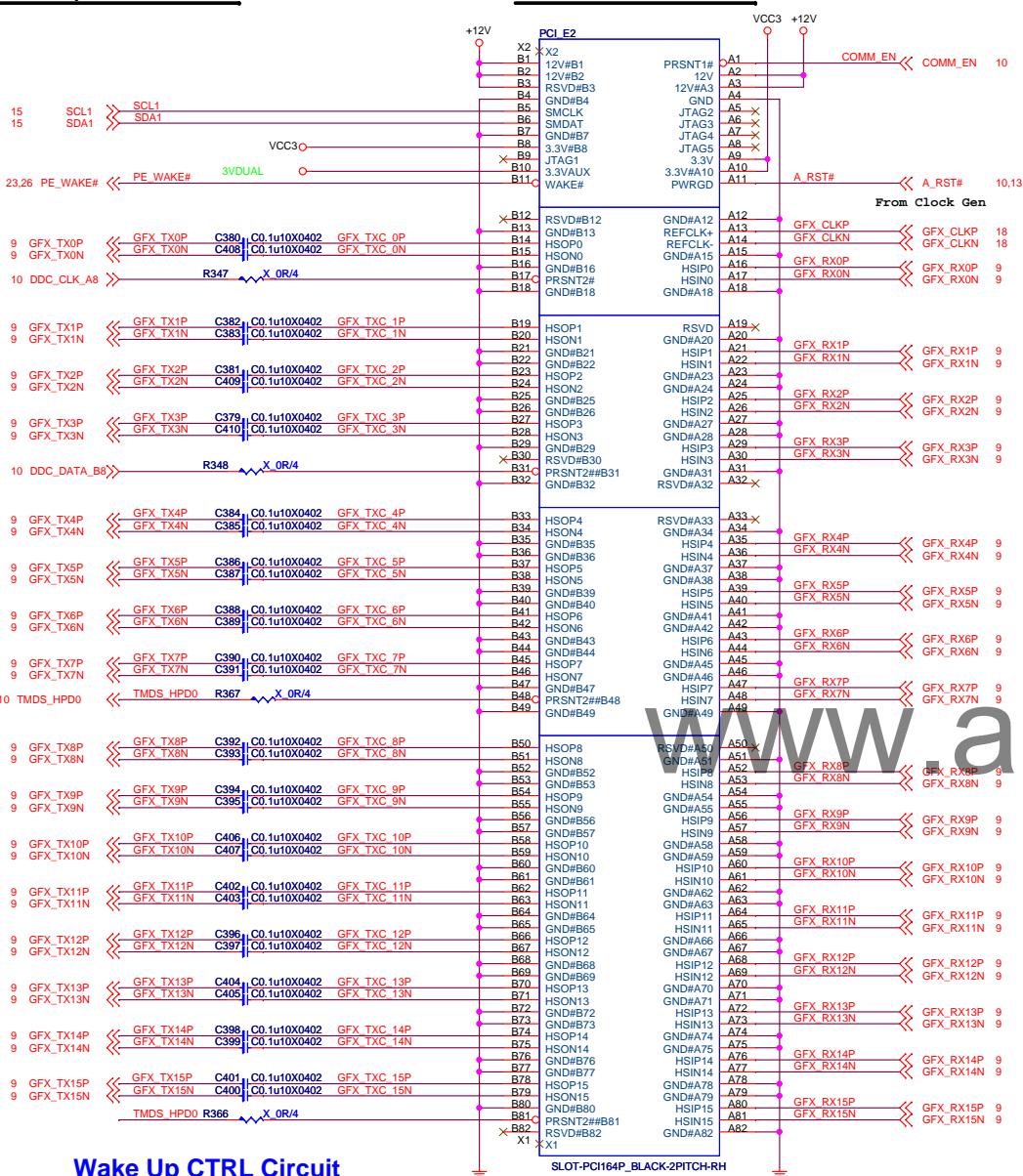
SB700 HAS 15K INTERNAL PU FOR PCI\_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

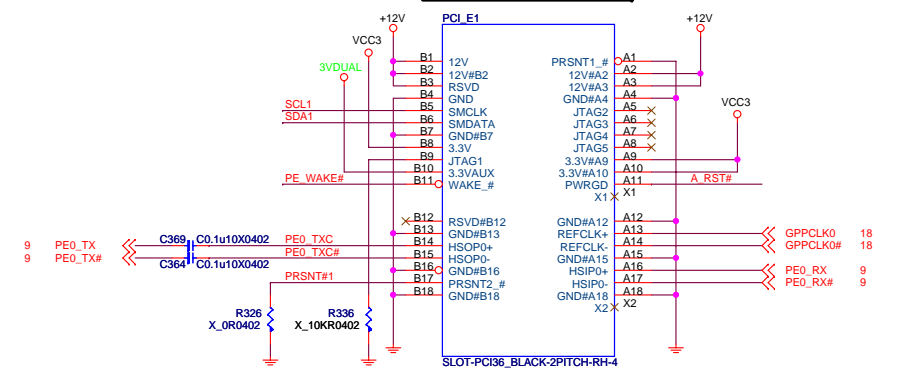


## PCI Express Slot x16/x1

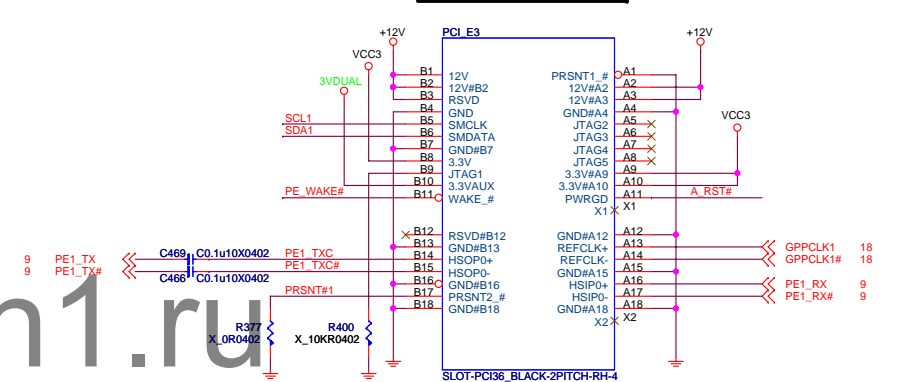
## PCI EXPRESS x16 Slot



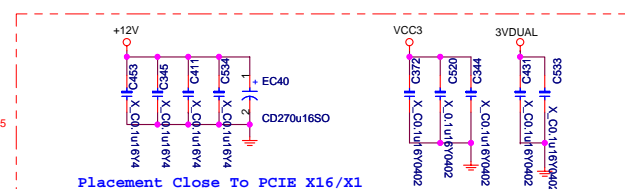
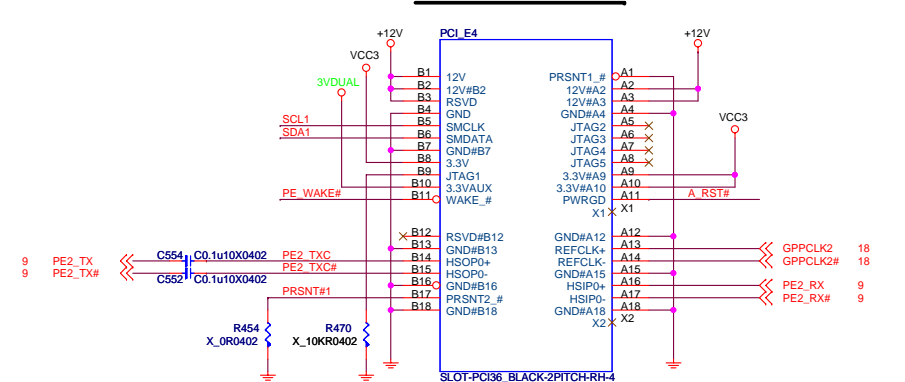
## PCI EXPRESS 1 Slot-1



## PCI EXPRESS 1 Slot-2

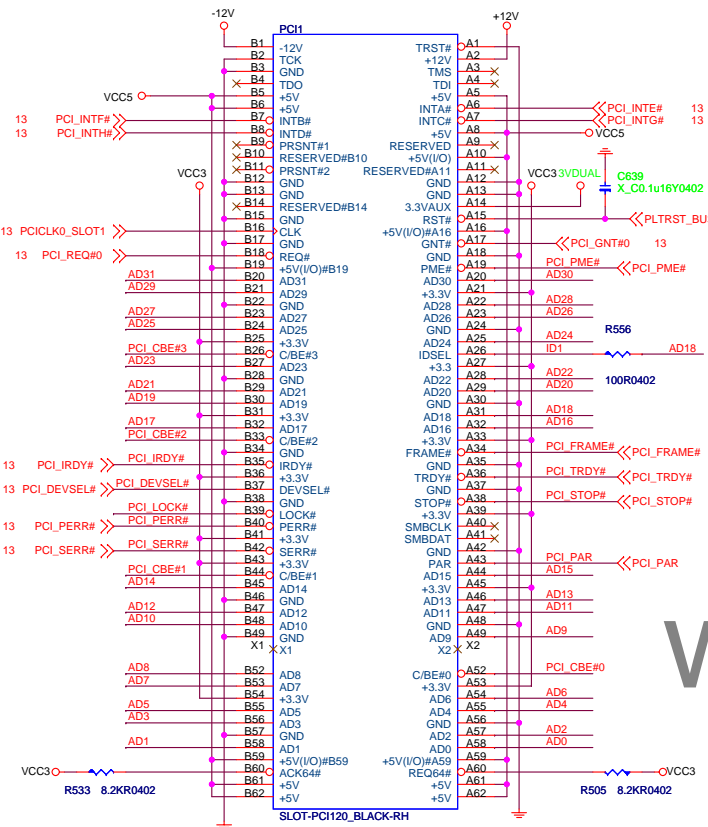


## PCI EXPRESS 1 Slot-3



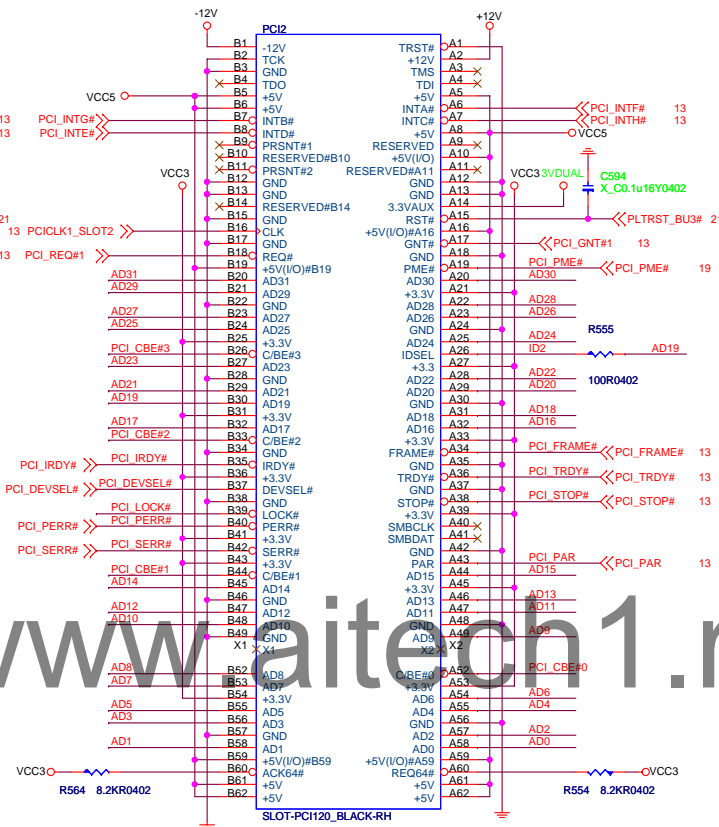
13 AD[31..0] >> AD[31..0]  
13 PCI\_CBE#[3..0] >> PCI\_CBE#[3..0]

### PCI SLOT 1 (PCI VER: 2.2 COMPLY)



IDSEL = AD18  
MASTER = PCI\_REQ#0  
PCI\_GNT#0

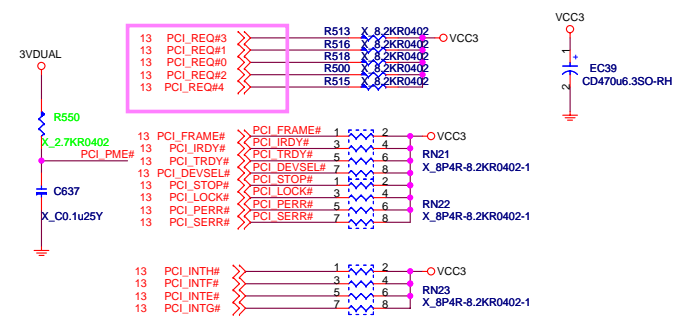
### PCI SLOT 2 (PCI VER: 2.2 COMPLY)



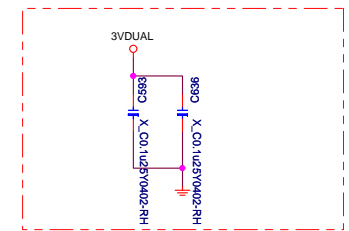
IDSEL = AD19  
MASTER = PCI\_REQ#1  
PCI\_GNT#1

IDSEL = AD20  
MASTER = PCI\_REQ#2  
PCI\_GNT#2

### PCI PULL-UP / DOWN RESISTORS



### PCI SLOT DECOUPLING CAPACITORS



**MSI**  
Link to the Future  
**MICRO-START INTL CO.,LTD.**

Title: **20 PCI Slot 1 & PCIE X 1 SLOT**

Size: Custom  
Document Number: **MS\_7699**  
Date: Friday, June 01, 2012

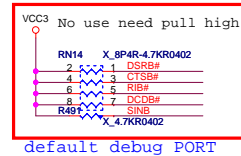
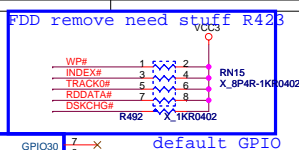
Rev: **0A**

Sheet 20 of 42

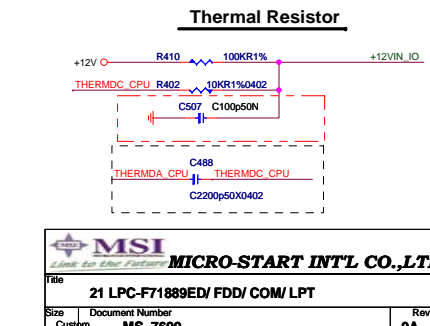
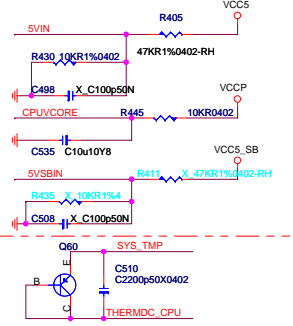
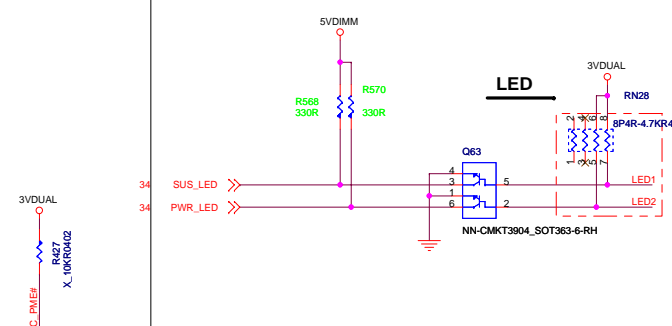
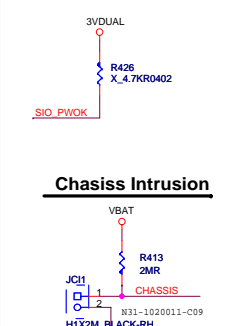
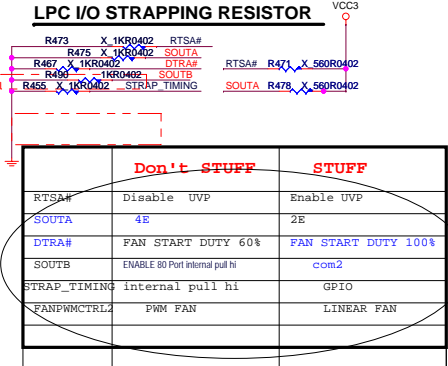
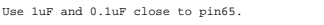
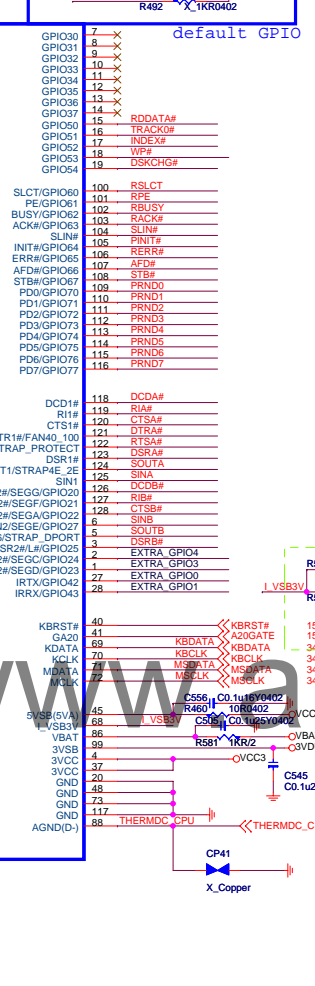
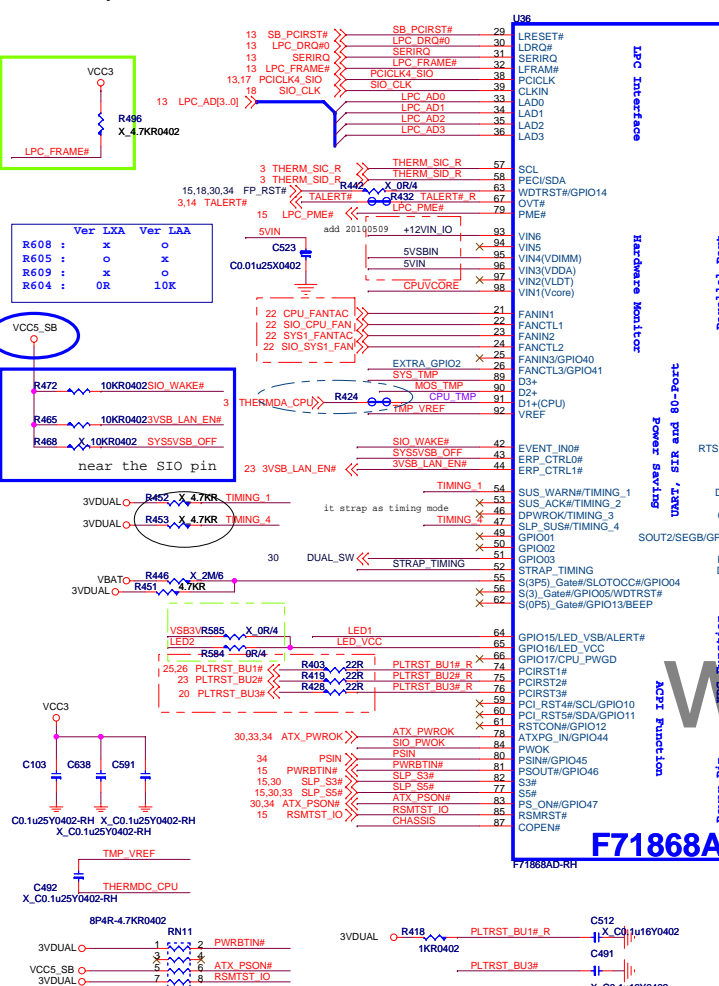
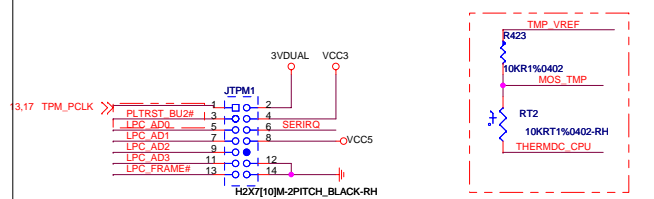
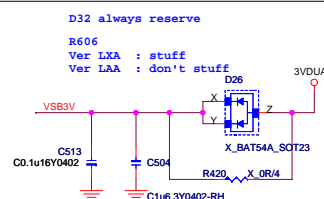
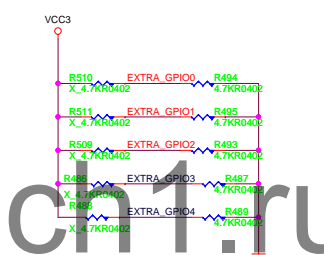
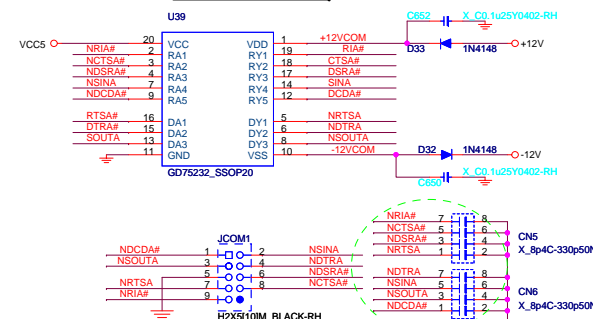
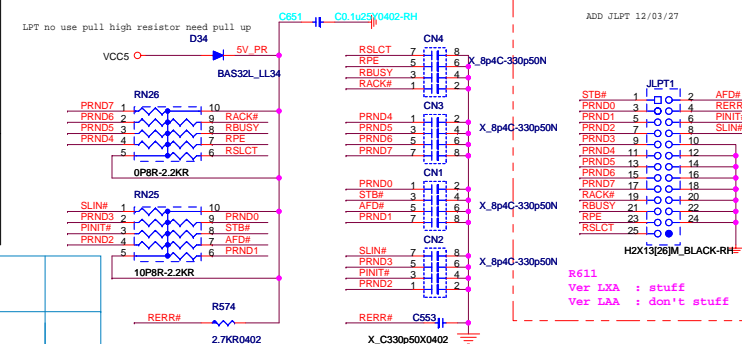


## Super I/O

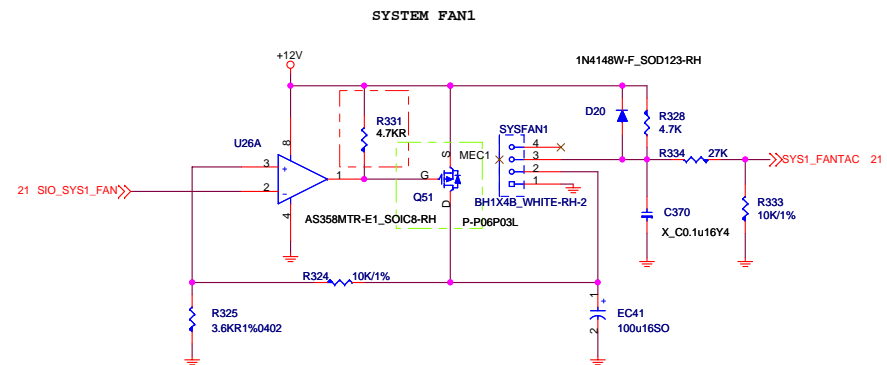
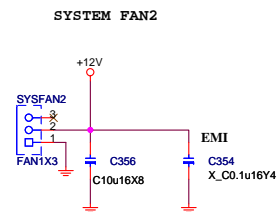
LPC SUPER I/O F71868AD COLAY F71878



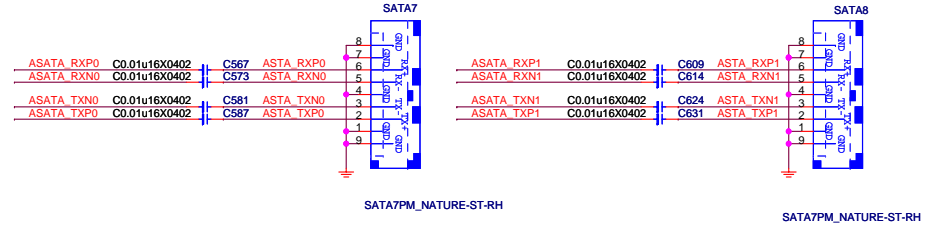
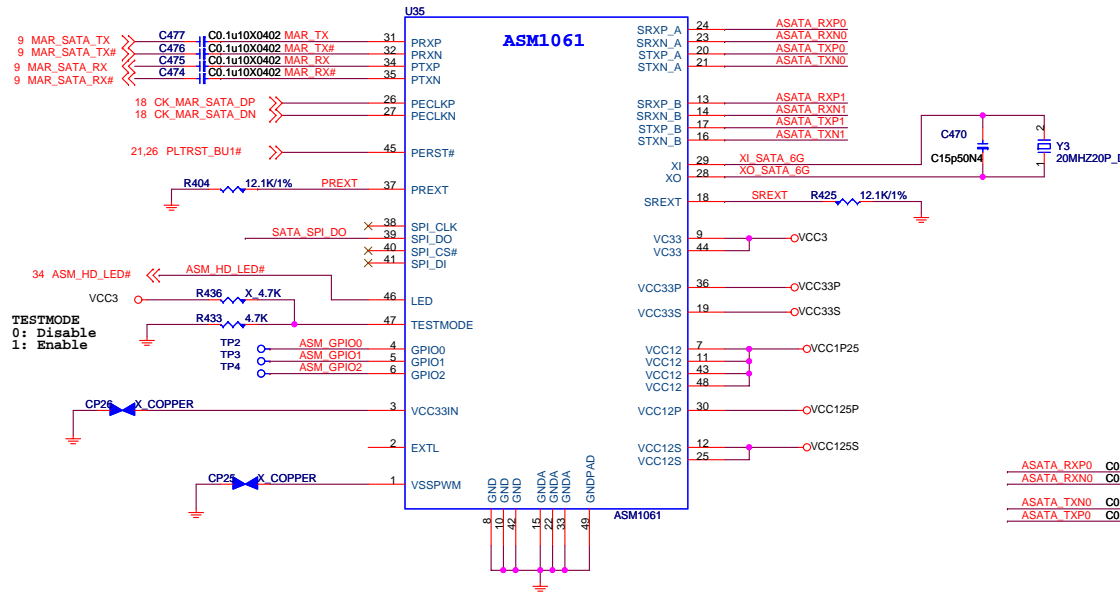
## PARALLAL PORT



### Type B : 4 PIN SYSTEM FAN FROM SIO (Smart Fan/DC MODE)







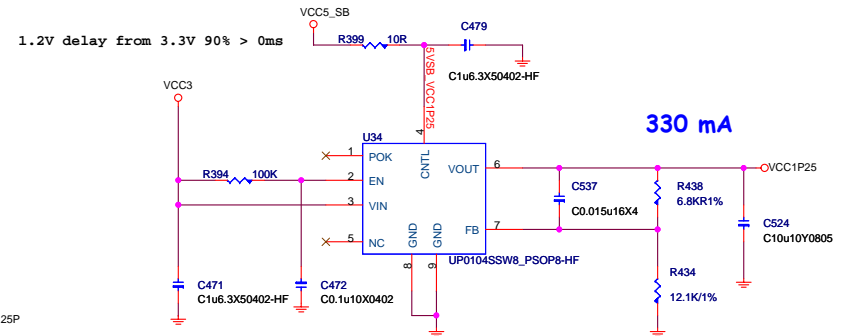
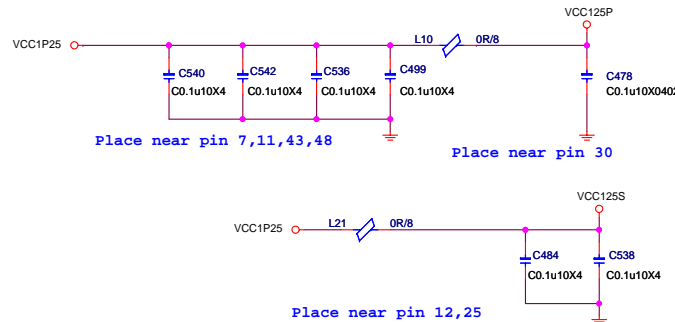
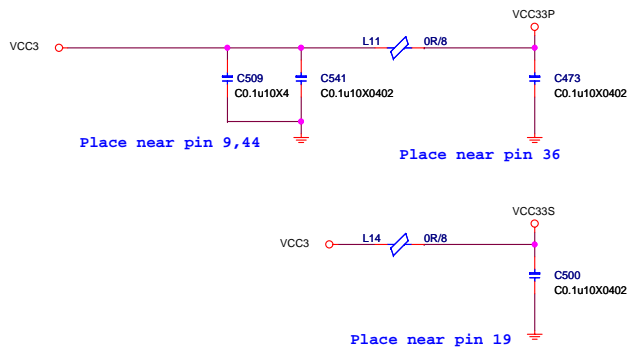
ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47

Add- 2011.3.18

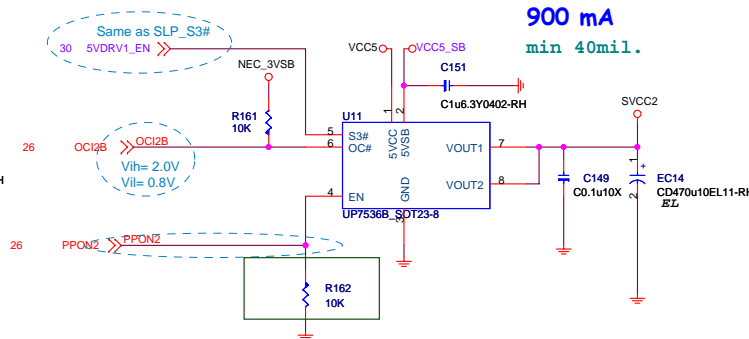
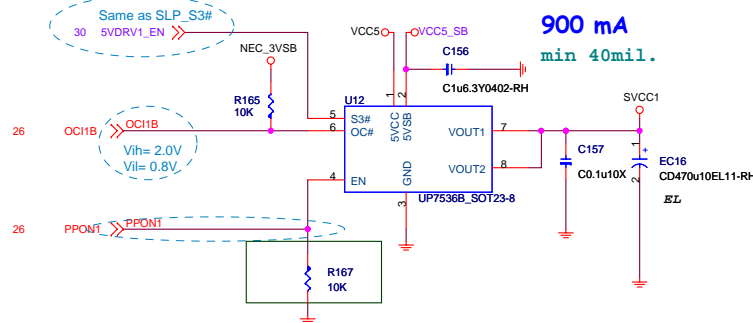
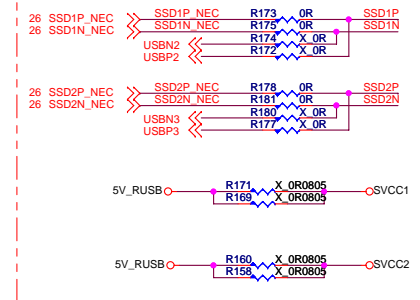
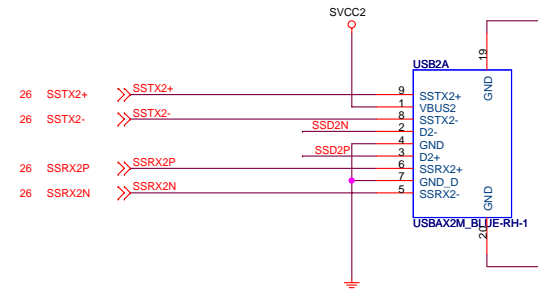
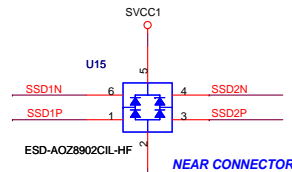
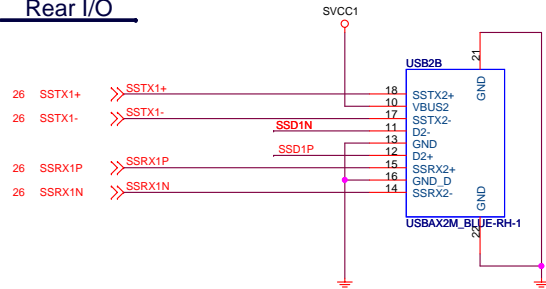
0: Spinup by H/W  
1: Spinup by S/W

SATA\_SPI\_DO don't need pull up (integrated pull-up)  
or pull down for Asmedia recommendation.  
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

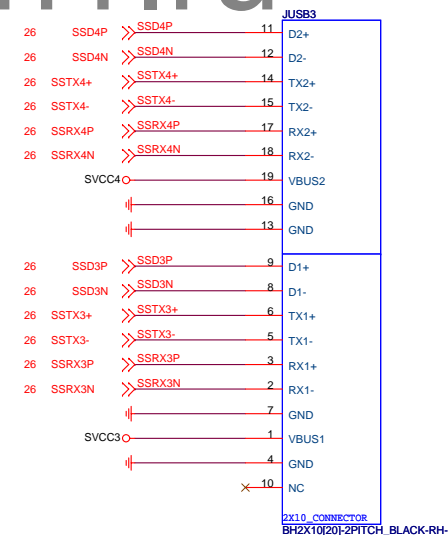
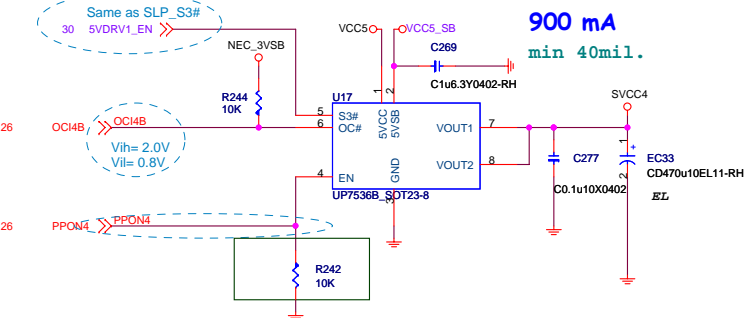
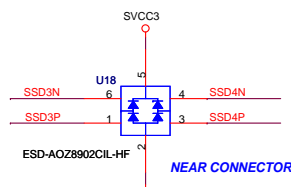
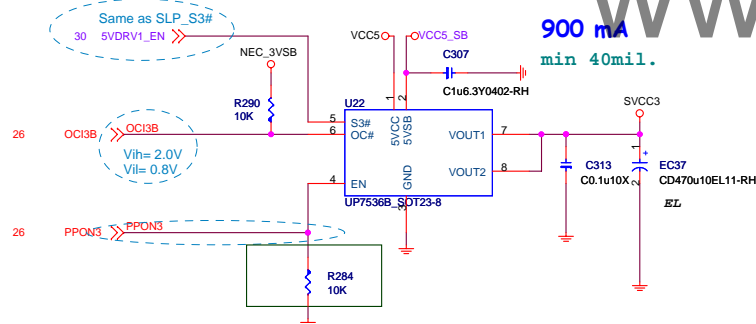




# Rear I/O



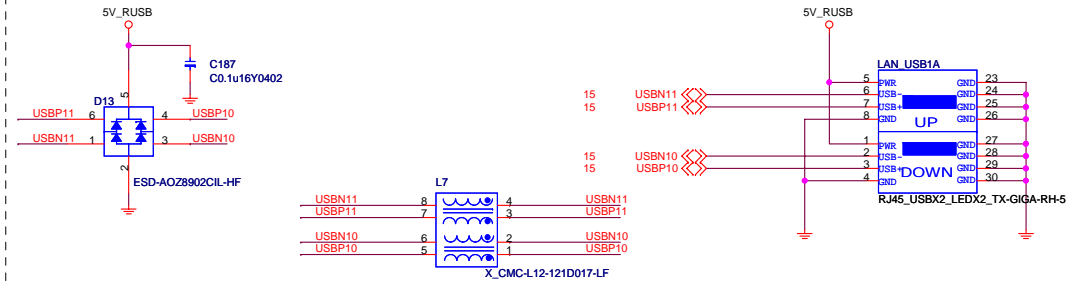
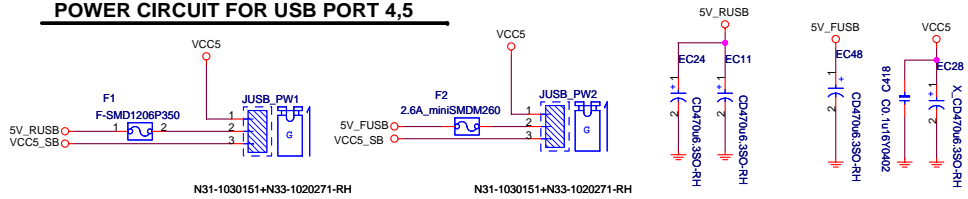
All power sources of uPD720200 are supplied, PPNx is enable.  
PPNx is low when OCx going to low.





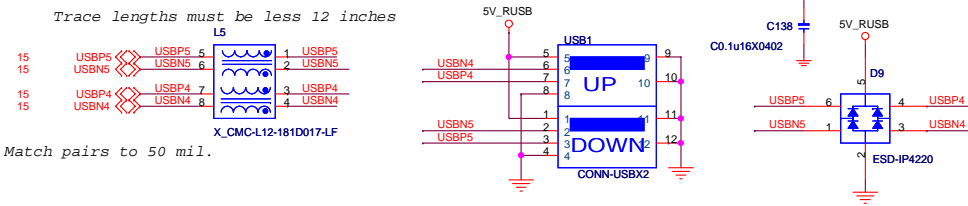


## POWER CIRCUIT FOR USB PORT 4,5

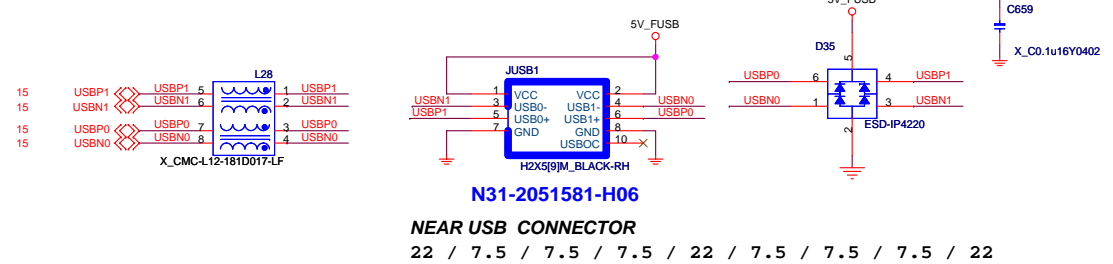


## REAR PANEL USB CONNECTOR FOR USB PORT 4,5

Trace lengths must be less 12 inches



## FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

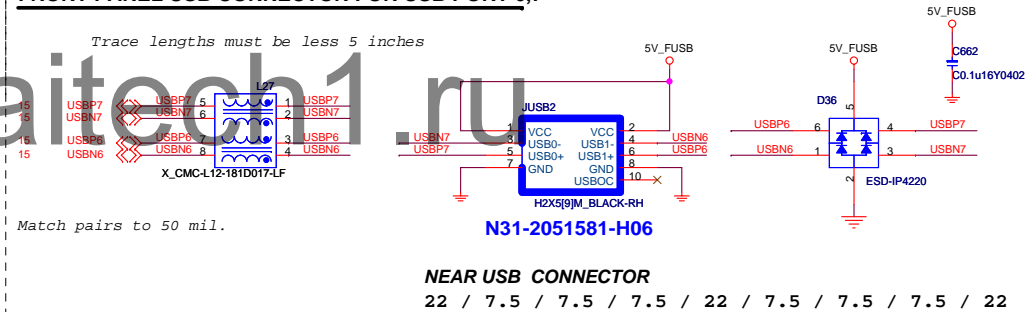


## REAR PANEL USB CONNECTOR FOR USB PORT 4,5

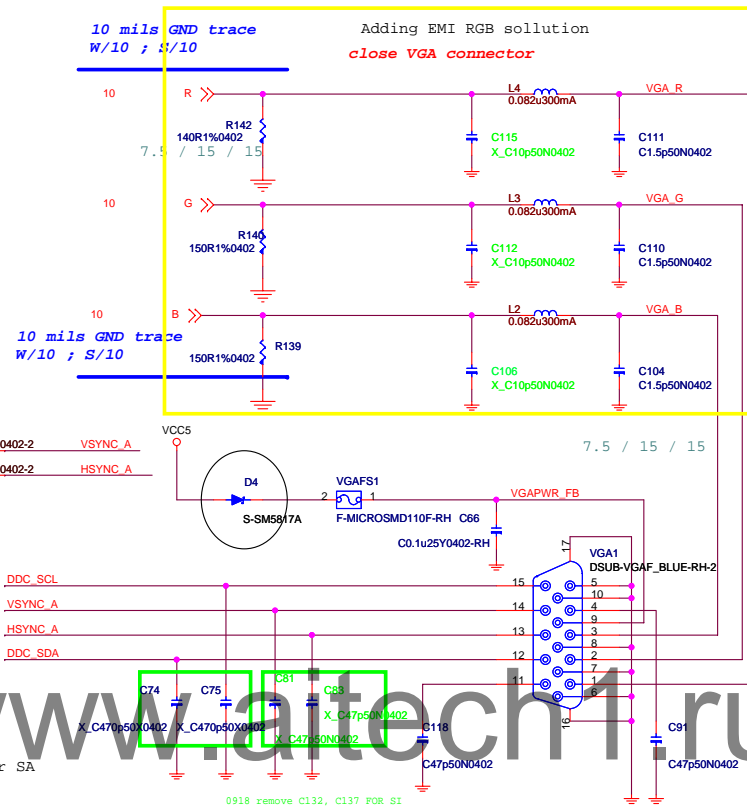
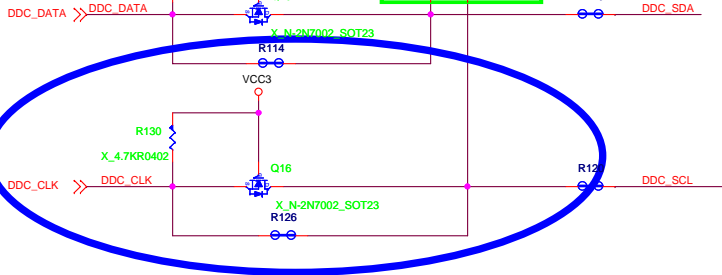
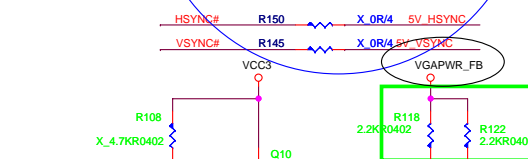
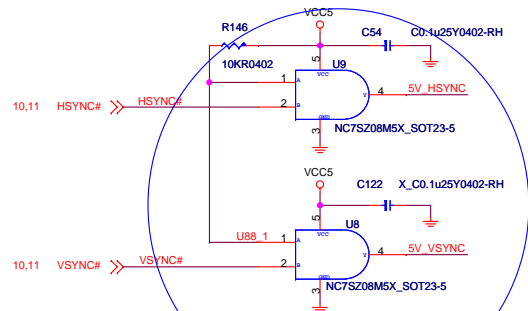
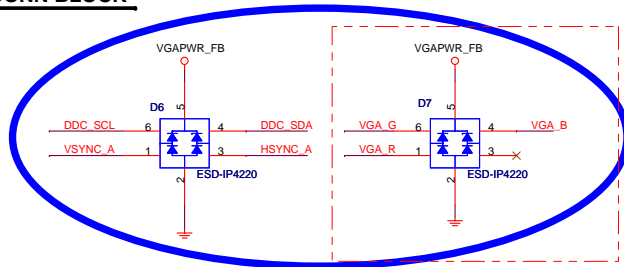


## FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

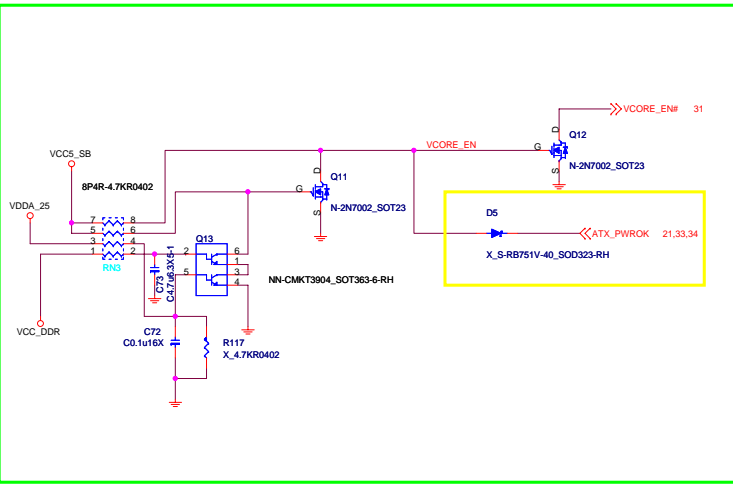
Trace lengths must be less 5 inches



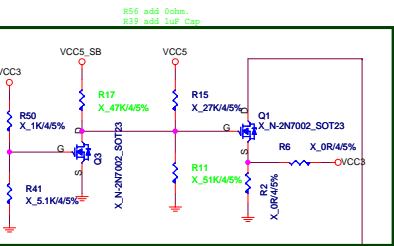
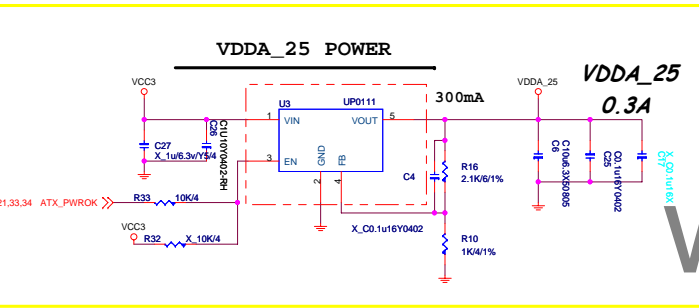
# VGA CONN BLOCK



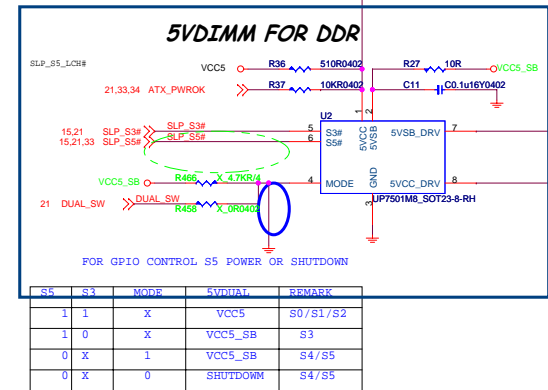
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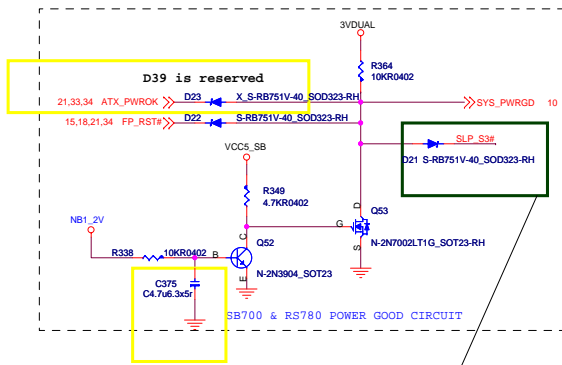
Chage 1087 to 7707 for Power up sequence



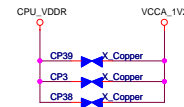
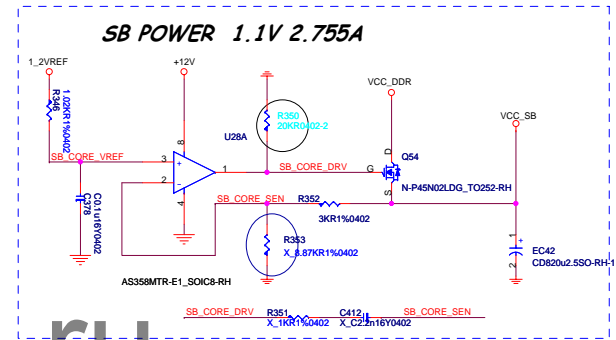
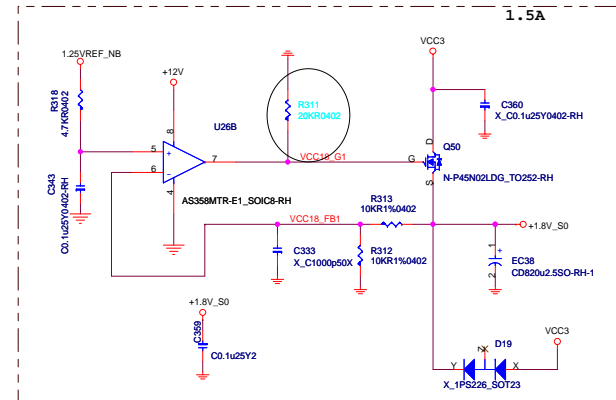
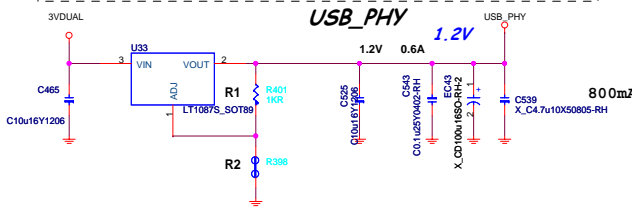
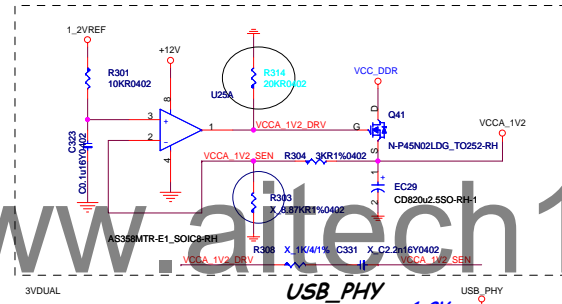
FIELD	OWN/DEM	COST DOWN
ADD	R597, R598, R599, Q56, R603	R601, R602, R600
REMOVE	R601, R602, R600	R597, R598, R599, Q56, R603
CHANGE	R602=C0.1u/16VY5V0402	R602=51Kohm/0402



S5	S3	MODE	5VDIMM	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWN	S4/S5

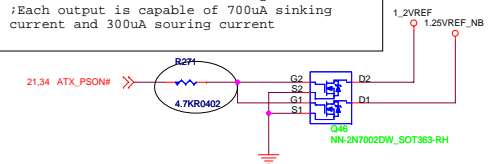


use Slp\_s3# control SYS\_PWRGD refer to AMD reference circuit

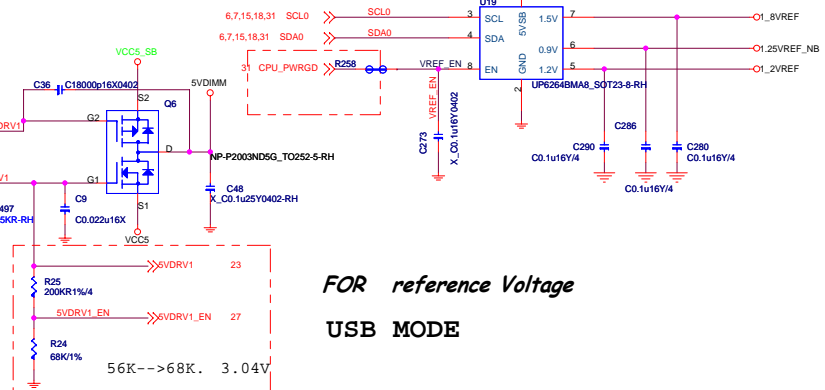


CPU\_VDDR 1.2V POWER  
CPU\_VDDR 1.2V 1.75A

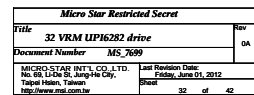
ADD R394 to increase the driving of 1.2VREF  
Each output is capable of 700uA sinking current and 300uA sourcing current



FOR reference Voltage  
USB MODE

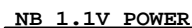




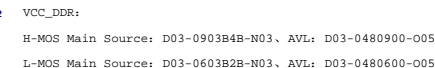
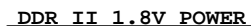




VCC5\_SB To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

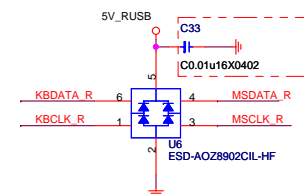


VCC1 1:RS780/RS760-1.1V RS740-1.2V

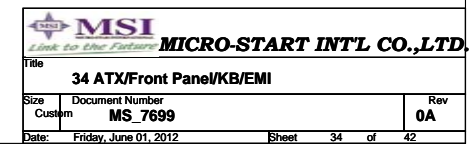


**VCC\_DDR**

## Intel Front Panel



## ATX Connector



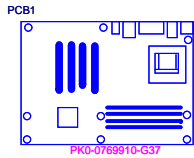
EMI solution

### Voltage test point

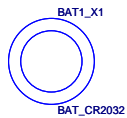
VCCP	□	VCCP
VCCP_NB	□	VCCP_NB
VCCA_1V2	□	VCCA_1V2
VCC_DDR	□	VCC_DDR
VDDA_25	□	VDDA_25
CPU_VDDR	□	CPU_VDDR
NB1_2V	□	NB1_2V
VCC1_1	□	VCC1_1
+1.8V_S0	□	1P8V_S0
USB_PHY	□	USB_PHY
VCC_SB	□	VCC_SB
5V_FUSB	□	5V_FUSB
5V_RUSB	□	5V_RUSB
LDOVDD	□	LDOVDD
VCC5_SB	□	VCC5_SB
3VDUAL	□	3VDUAL
VCC3	□	VCC3
VTT_DDR	□	VTT_DDR
+12V	□	12V
5VDIMM	□	5VDIMM
VCC5	□	VCC5
LAN_VDD1.05	□	LAN_VDD1P05
+12VIN	□	12VIN
VCC1P25	□	VCC1P25
NEC_3VSB	□	NEC_3VSB
VCC_1P05	□	VCC_1P05
SVCC1	□	SVCC1
SVCC2	□	SVCC2
SVCC3	□	SVCC3
SVCC4	□	SVCC4

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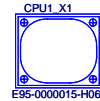
PCB



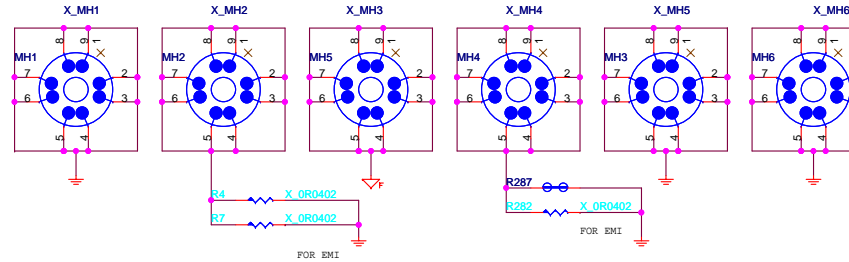
BATTERY



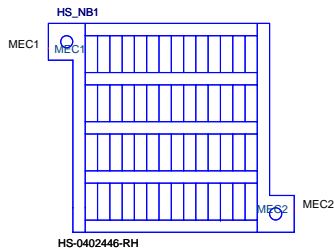
CPU RM



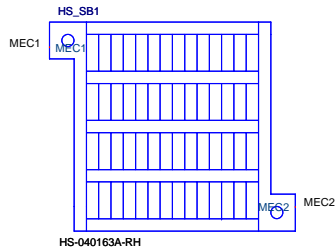
Mounting Holes



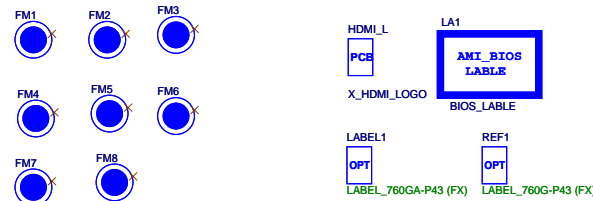
NB HEATSINK



SB HEATSINK



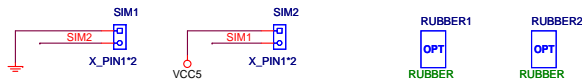
Optics Orientation Holes

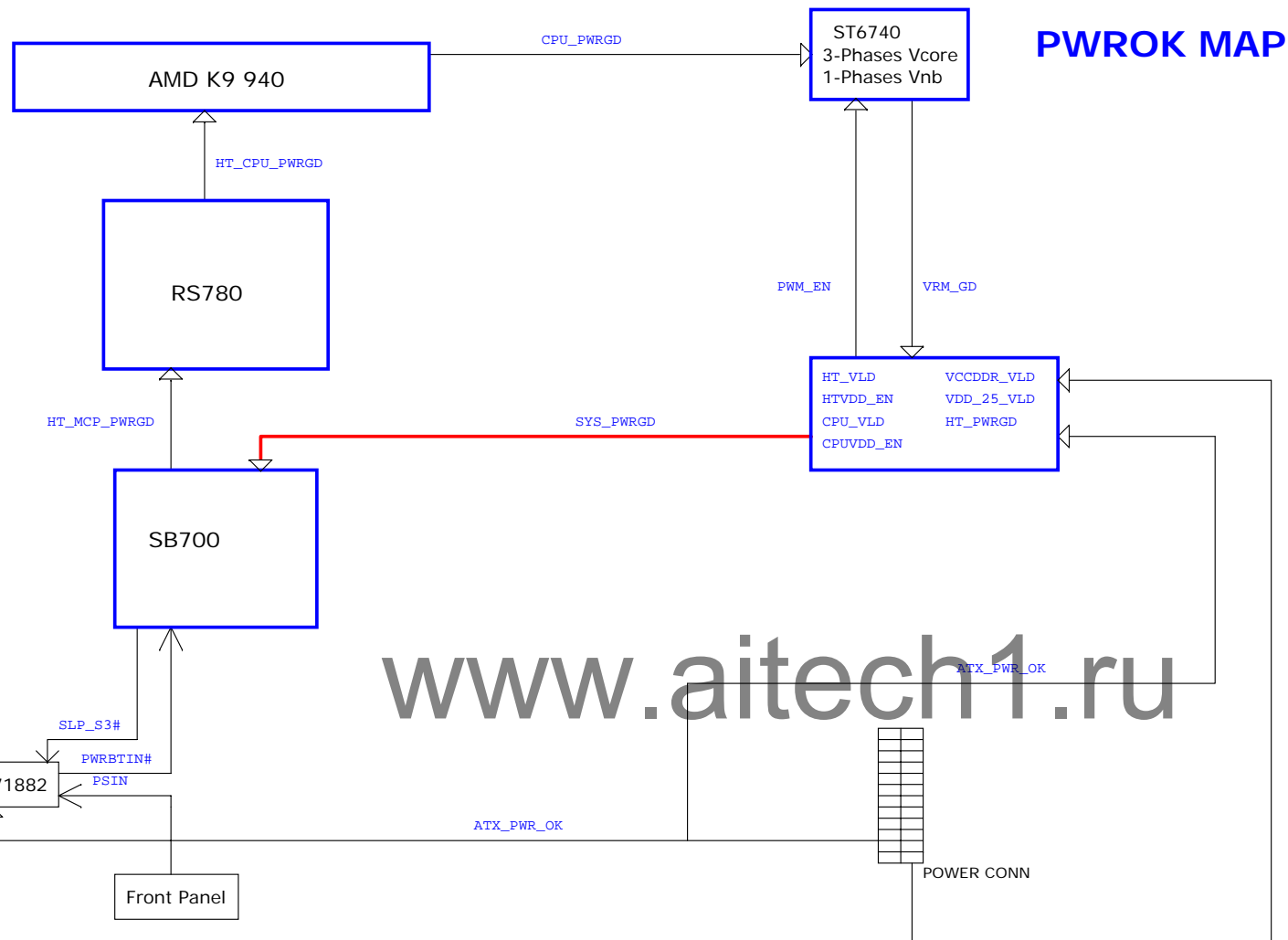


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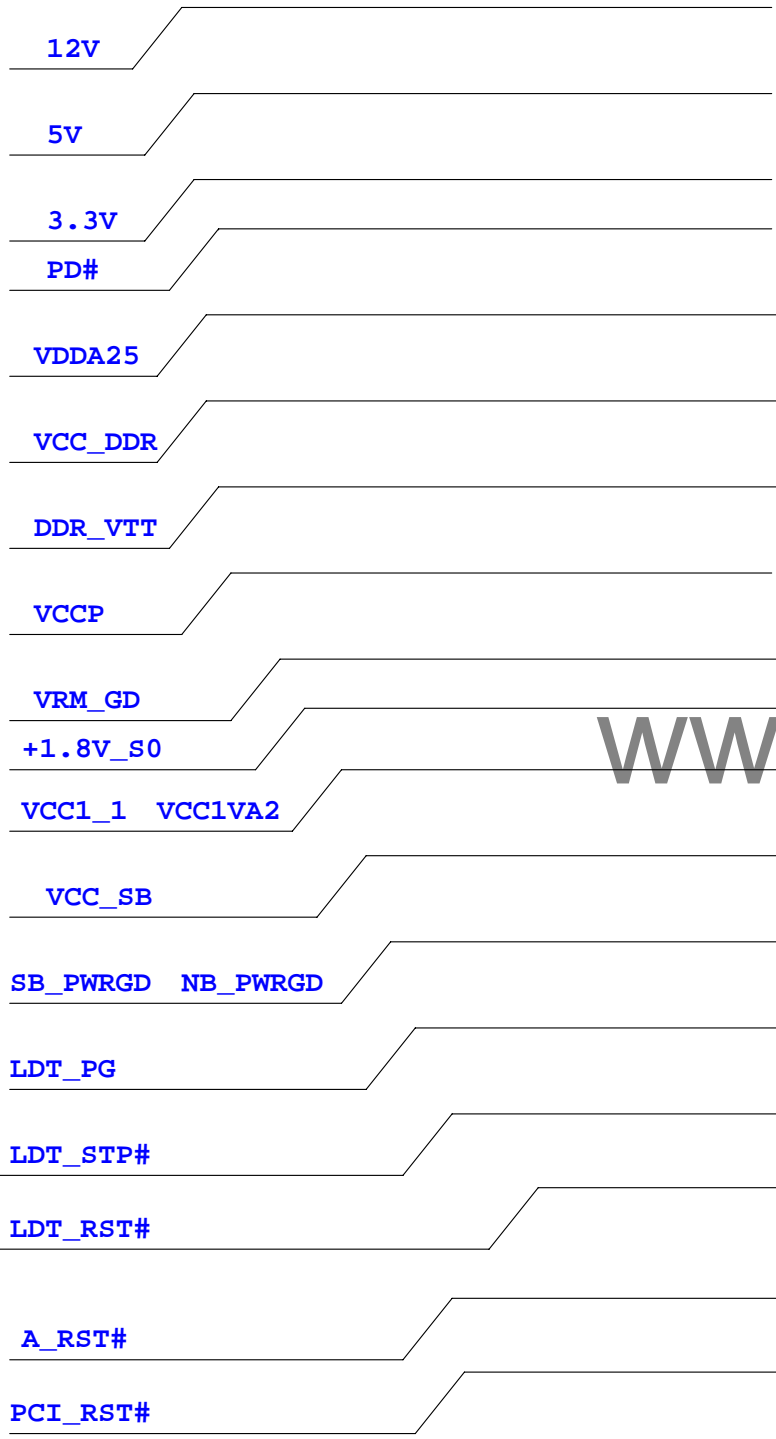
EL-CAP USED BY CFG\_2331\_816GH.

Simulation






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## SB700/750 GPIO Config

[illegible]

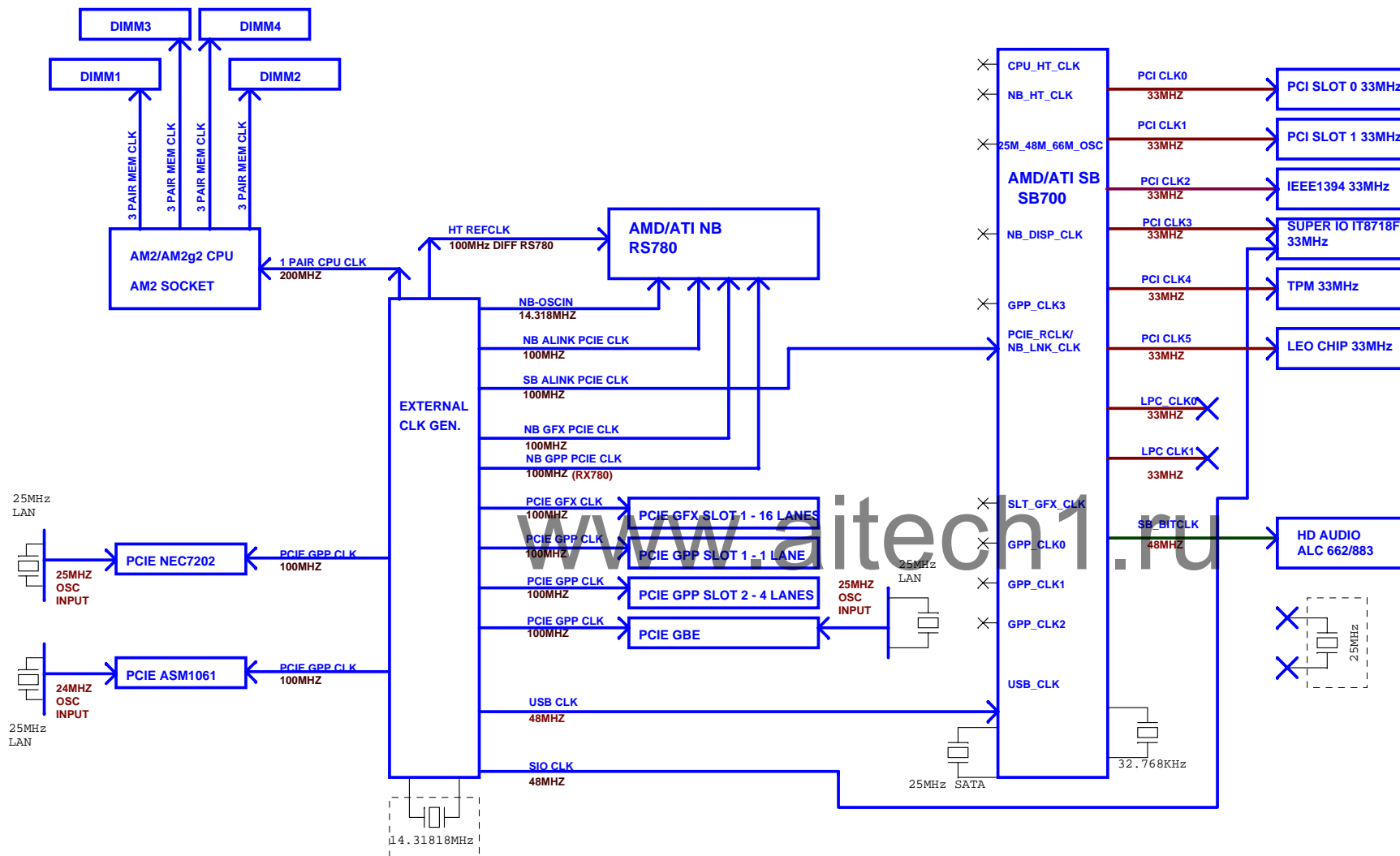
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INT# PCI_INTH# PCI_INT#	PREQ#1 PGNT#1	AD22	PCICLK1


**MSI**  
*Link to the Future*

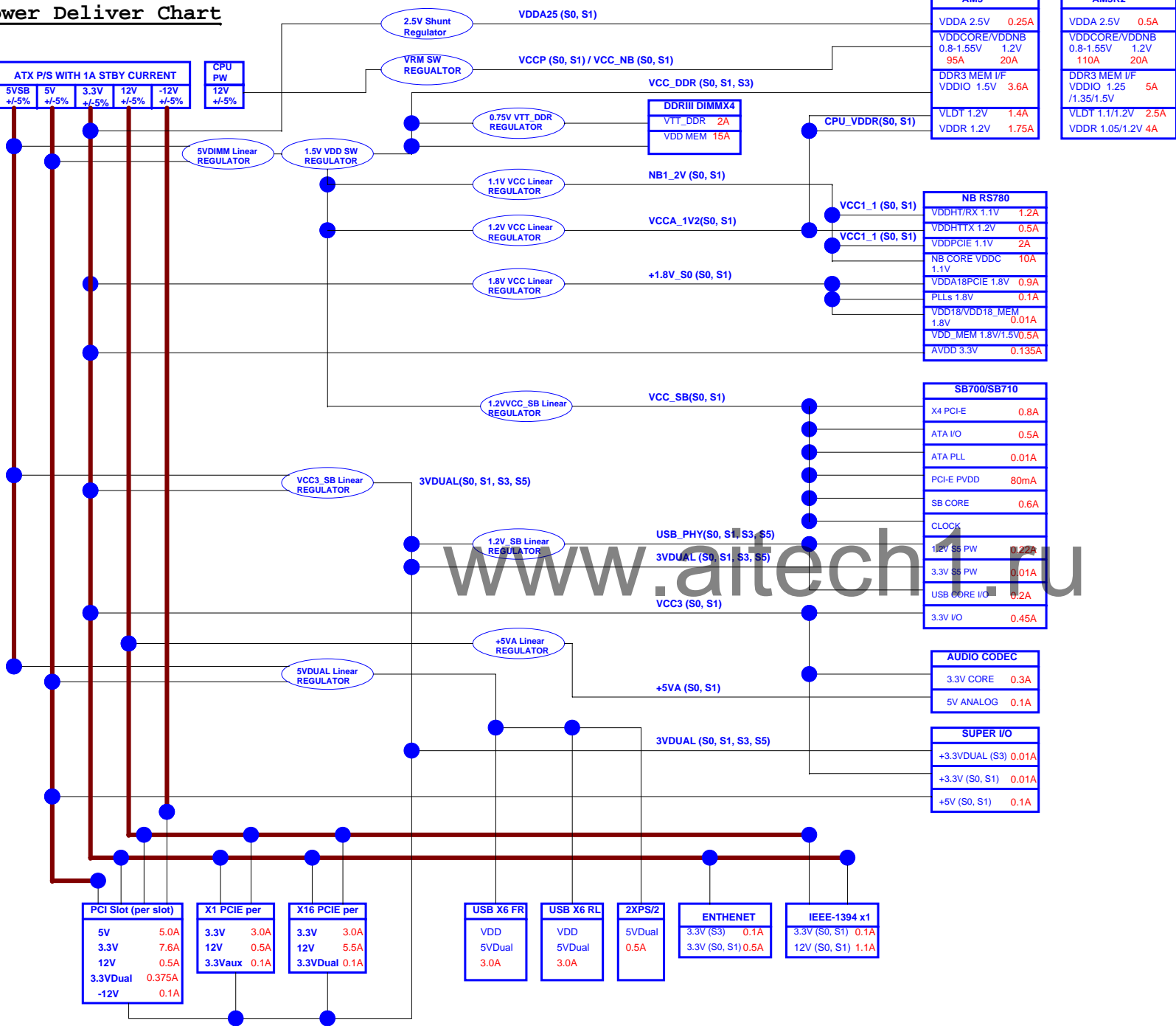
**MICRO-START INT'L CO., LTD.**  
 Title: **39 GPIO Configuration**

Size	Document Number	Rev
Custom	<b>MS_7699</b>	<b>0A</b>
Date:	Friday, June 01, 2012	Sheet: 36 of 42





Power Deliver Chart



MS-7699-0A

- Base on 7641-3.1
- 1.2DIMM change to 4DIMM
  - 2.Slot update:1\*PCIE16X/2\*PCIE1X/3X PCI
  - 3.Print Port Pinheader use latest N31-2131131-H06
  - 4.F71869AD change to F71868AD

- 2012/03/26
- 1.power solution change to 4+1 H:2,L:2 125 support
  - 2.clock gen change to ICS/9LPRS477DKLFT
  - 3.Add usb 3.0 4port NEC7202
  - 4.Add SATA 6G ASM1061
  - 5:Change AUDIO to 3 port

- 2012/03/29
- 1:add 1 PCIE x1
  - 2:reduce 1PCI slot 3
  - 3:reduce buzzer

- 2012/05/27
- 1:add R552/583/584/585 for F71868 colay F71878
  - 2:change vccp 5020 CAP
  - 3:Add EMI memory solution

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